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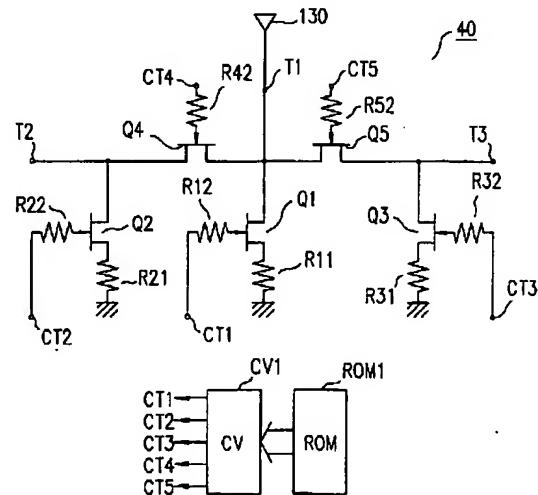
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(54)【発明の名称】スイッチアッテネータ

(57)【要約】

【課題】高周波機器に使用される高周波スイッチおよびアッテネータ回路において、機器の小型化、低コスト化を実現する。

【解決手段】第1状態において、第1端子は、第2端子に接続され、第1端子は、第3端子から遮断され、第3端子は、グラウンドに接続され、第1端子からみたインピーダンスZ1が第2端子からみたインピーダンスZ2に実質的に等しい関係を維持しつつ、第1端子および第2端子の間の減衰量を変化させるように、スイッチアッテネータは電気的に制御可能であり、第2状態において、第1端子は、第3端子に接続され、第1端子は、第2端子から遮断され、第2端子は、グラウンドに接続され、第1端子からみたインピーダンスZ1が第3端子からみたインピーダンスZ3に実質的に等しい関係を維持しつつ、第1端子および第3端子の間の減衰量を変化させるように、スイッチアッテネータは電気的に制御可能である。



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【特許請求の範囲】

【請求項1】 アンテナに接続される第1端子と、送信機に接続される第2端子と、受信機に接続される第3端子とを備え、第1状態および第2状態を切り替えるスイッチアッテネータであって、

該第1状態において、

該第1端子は、該第2端子に接続され、

該第1端子は、該第3端子から遮断され、

該第3端子は、グラウンドに接続され、

該第1端子からみたインピーダンスZ1が該第2端子からみたインピーダンスZ2に実質的に等しい関係を維持しつつ、該第1端子および該第2端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、

該第2状態において、

該第1端子は、該第3端子に接続され、

該第1端子は、該第2端子から遮断され、

該第2端子は、グラウンドに接続され、

該第1端子からみたインピーダンスZ1が該第3端子からみたインピーダンスZ3に実質的に等しい関係を維持しつつ、該第1端子および該第3端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であるスイッチアッテネータ。

【請求項2】 第1トランジスタが、前記第1端子とグラウンドとの間に設けられ、

第2トランジスタが、前記第2端子とグラウンドとの間に設けられ、

第3トランジスタが、前記第3端子とグラウンドとの間に設けられ、

第4トランジスタが、該第1端子と該第2端子との間に設けられ、

第5トランジスタが、該第1端子と該第3端子との間に設けられており、

前記第1状態において、

該第3トランジスタは、オン状態であり、

該第5トランジスタは、オフ状態であり、

前記第2状態において、

該第3トランジスタは、オン状態であり、

該第5トランジスタは、オフ状態である、請求項1に記載のスイッチアッテネータ。

【請求項3】 前記インピーダンスZ1は、 $0.5 \times Z_A \sim 2.0 \times Z_A$ の範囲に実質的に含まれ、

前記インピーダンスZ2は、 $0.5 \times Z_T \sim 2.0 \times Z_T$ の範囲に実質的に含まれ、

前記インピーダンスZ3は、 $0.5 \times Z_R \sim 2.0 \times Z_R$ の範囲に実質的に含まれ、

ここでZA、ZTおよびZRは、それぞれ前記アンテナ、前記送信機および前記受信機のインピーダンスを表す請求項1に記載のスイッチアッテネータ。

【請求項4】 前記第1トランジスタ、前記第2トラン

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ジスタ、前記第3トランジスタ、前記第4トランジスタ

および前記第5トランジスタのそれぞれは、ドレインと、ソースと、2つのゲートとを有するデュアルゲート電界効果トランジスタであり、該2つのゲートの一方のゲートは、該ドレインに接続されており、該2つのゲートの他方のゲートは、該ソースに接続されており、該2つのゲートは、それぞれ抵抗を介して電気的な制御のための電圧を受け取る請求項3に記載のスイッチアッテネータ。

【請求項5】 第1アンテナに接続される第1端子と、送信機に接続される第2端子と、受信機に接続される第3端子と、第2アンテナに接続される第4端子とを備え、第1状態、第2状態、第3状態および第4状態を切り替えるスイッチアッテネータであって、

該第1状態においては、

該第1端子は、該第2端子に接続され、かつ該第3端子から遮断され、

該第3端子は、グラウンドに接続され、

該第4端子は、該第1端子、該第2端子、該第3端子および該グラウンドから遮断され、

該第1端子からみたインピーダンスZ1が該第2端子からみたインピーダンスZ2に実質的に等しい関係を維持しつつ、該第1端子および該第2端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、

該第2状態においては、

該第1端子は、該第3端子に接続され、かつ該第2端子から遮断され、

該第2端子は、グラウンドに接続され、

該第4端子は、該第1端子、該第2端子、該第3端子および該グラウンドから遮断され、

該第1端子からみたインピーダンスZ1が該第3端子からみたインピーダンスZ3に実質的に等しい関係を維持しつつ、該第1端子および該第3端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、

該第3状態においては、

該第4端子は、該第2端子に接続され、かつ該第3端子から遮断され、

該第3端子は、グラウンドに接続され、

該第1端子は、該第2端子、該第3端子、該第4端子および該グラウンドから遮断され、

該第4端子からみたインピーダンスZ4が該第2端子からみたインピーダンスZ2に実質的に等しい関係を維持しつつ、該第4端子および該第2端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、

該第4状態においては、

該第4端子は、該第3端子に接続され、かつ該第2端子から遮断され、

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該第2端子は、グラウンドに接続され、
該第1端子は、該第2端子、該第3端子、該第4端子および該グラウンドから遮断され、
該第4端子からみたインピーダンスZ4が該第3端子からみたインピーダンスZ3に実質的に等しい関係を維持しつつ、該第4端子および該第3端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であるスイッチアッテネータ。

【請求項6】 第1トランジスタが、前記第1端子とグラウンドとの間に設けられ、

第2トランジスタが、前記第2端子とグラウンドとの間に設けられ、

第3トランジスタが、前記第3端子とグラウンドとの間に設けられ、

第4トランジスタが、該第1端子と該第2端子との間に設けられ、

第5トランジスタが、該第1端子と該第3端子との間に設けられ、

第6トランジスタが、前記第4端子とグラウンドとの間に設けられ、

第7トランジスタが、該第2端子と該第4端子との間に設けられ、

第8トランジスタが、該第3端子と該第4端子との間に設けられ、

前記第1状態において、

該第3トランジスタは、オン状態であり、

該第5トランジスタ、該第6トランジスタ、該第7トランジスタおよび該第8トランジスタは、オフ状態であり、

前記第2状態において、

該第2トランジスタは、オン状態であり、

該第4トランジスタ、該第6トランジスタ、該第7トランジスタおよび該第8トランジスタは、オフ状態であり、

前記第3状態において、

該第3トランジスタは、オン状態であり、

該第1トランジスタ、該第4トランジスタ、該第5トランジスタおよび該第8トランジスタは、オフ状態であり、

前記第4状態において、

該第2トランジスタは、オン状態であり、

該第1トランジスタ、該第4トランジスタ、該第5トランジスタおよび該第7トランジスタは、オフ状態である、請求項5に記載のスイッチアッテネータ。

【請求項7】 前記インピーダンスZ1およびZ4は、 $0.5 \times Z_A \sim 2.0 \times Z_A$ の範囲に実質的に含まれ、前記インピーダンスZ2は、 $0.5 \times Z_T \sim 2.0 \times Z_T$ の範囲に実質的に含まれ、

前記インピーダンスZ3は、 $0.5 \times Z_R \sim 2.0 \times Z_R$ の範囲に実質的に含まれ、

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ここでZA、ZTおよびZRは、それぞれ前記アンテナ、前記送信機および前記受信機のインピーダンスを表す請求項5に記載のスイッチアッテネータ。

【請求項8】 半導体基板上に集積化されて形成されている請求項1から請求項7のいずれかに記載のスイッチアッテネータ。

【請求項9】 電力増幅器をさらに備えており、該電力増幅器は、前記半導体基板上に集積化されて形成されている請求項8に記載のスイッチアッテネータ。

10 【請求項10】 低雑音増幅器をさらに備えており、該低雑音増幅器は、前記半導体基板上に集積化されて形成されている請求項9に記載のスイッチアッテネータ。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】 本発明は高周波送受信回路に使用される高周波スイッチおよび高周波アッテネータを含むスイッチアッテネータに関する。また本発明は、このスイッチアッテネータを実現する半導体デバイスと、この半導体デバイスを用いた高周波機器とも関する。

20 【0002】

【従来の技術】 図1は、従来の技術による送受信回路の高周波（以下「RF」とする）部10を示すブロック図である。送受信回路のRF部10は、RFスイッチ120を備えており、これにより送信および受信を選択的におこなう。送信時には、変調信号入力端子（MOD in）110において入力された信号は、周波数変換器（以下「ミキサ」とする）112、可変利得増幅器（以下「AGCアンプ」とする）114、電力増幅器（PA）116、RFスイッチ（RF SW）120および

30 周波数フィルタ122を通ってアンテナ130から空間へ輻射される。

【0003】 逆に受信時には、アンテナ130において受け取られた信号は、周波数フィルタ122、RFスイッチ120、減衰器150、低雑音増幅器（LNA）152およびミキサ154を通って中間周波（以下「IF」とする）信号出力端子（IF out）156から出力される。

【0004】 送受信いずれの場合も、フェーズロックループ（以下「PLL」とする）170および発振器172は、所望の周波数をもつ局部発振信号を発生し、信号分配器（DIV）174に出力する。ミキサ112は、変調信号および局部発振信号を混合することによって、RF信号を生成し、AGCアンプ114に出力する。ミキサ154は、RF信号および局部発振信号を混合することによって、IF信号を生成し、IF信号出力端子156に出力する。

【0005】 図1のRF部10の動作を以下に説明する。RF部10は、例えば携帯電話の端末機に代表される移動体通信機の一部である。移動体通信機においては、機器構成の簡略化のために、比較的、大きな体積を

要するアンテナ130（ここでは周波数フィルタ122も含めて考える）は、ほとんどの場合において送信回路および受信回路の双方のために使用される。アンテナ部を送受信で共用するために送信時ににおいては、アンテナ130は、電力増幅器116に電気的に結合され、かつ低雑音増幅器152から電気的に分離される。逆に受信時においては、アンテナ130は、電力増幅器116から電気的に分離され、かつ低雑音増幅器152に電気的に結合される。このような送受信のための切替をおこなうために、通常、半導体素子化されたRFスイッチ120が採用される。従来技術によるRFスイッチ120は、スイッチング素子としてトランジスタを用いており、トランジスタがオン状態およびオフ状態のいずれかの状態をとるよう電気的に制御している。

【0006】また移動体通信における端末機（例えば携帯電話のハンドセットそのもの）は、最寄りの基地局にRF信号を送信し、基地局からRF信号を受信することによって通信をおこなう。基地局において受信される電力をほぼ一定に維持するために、端末機と基地局との距離に応じて、端末機から送信される電力を微妙に制御する必要がある。反対に端末機のIF信号出力端子156において出力される電力をほぼ一定に維持するためには、低雑音増幅器152に入力されるRF電力を制御する必要がある。これらの要求を満たすため端末機のRF部10は一般に、送信のためのAGCアンプ114と、受信のためのアッテネータ150とを備えている。

【0007】図2は、従来の技術によるスイッチ20の回路図である。図2において、スイッチ20は、電界効果トランジスタ（以下「FET」とする）200～203、インピーダンス調整用抵抗器210および211、ゲートバイアス抵抗器220～223、アンテナ端子230、送信電力入力端子231、受信電力出力端子232、第1制御端子245および第2制御端子246を備えている。

【0008】図2のスイッチの動作を説明する。送信時には、FET201および202の閾値の絶対値より大きい負の電圧を第2制御端子246に印加することによって、FET201および202をオフ状態にし、かつゼロまたは正の電圧を第1制御端子245に印加し、FET200および203をオン状態にする。これにより、送信電力は、端子231、FET200およびアンテナ端子230を通って、アンテナ250に出力される。

【0009】逆に受信時には、FET200および203の閾値の絶対値より大きい負の電圧を第1制御端子245に印加することによって、FET200および203をオフ状態にし、かつゼロまたは正の電圧を第2制御端子246に印加してFET201および202をオン状態にする。これにより、受信電力は、アンテナ250、端子230およびFET201を通って、端子23

2に出力される。

【0010】

【発明が解決しようとする課題】携帯電話の移動端末機器においては、携帯性を高めるため機器を小型・軽量化するとともに、低コスト化することが重要である。これを実現するために現在、RF部における回路の小型化および低コスト化が強く求められている。ところが上述のいずれの従来技術においても、送受信回路は、スイッチ、AGCアンプおよびアッテネータを別個に備えることが必要であった。その結果、従来の技術による送受信回路は、機器のサイズおよびコストの増大が不可避であるという課題を有していた。

【0011】本発明は、上記課題を解決するためになされたものであり、その目的とするところは、高周波送受信回路に用いられる小型・軽量および低コストな、スイッチおよびアッテネータとして機能する装置を提供することにある。

【0012】

【課題を解決するための手段】本発明によるスイッチアッテネータは、アンテナに接続される第1端子と、送信機に接続される第2端子と、受信機に接続される第3端子とを備え、第1状態および第2状態を切り替えるスイッチアッテネータであって、該第1状態において、該第1端子は、該第2端子に接続され、該第1端子は、該第3端子から遮断され、該第3端子は、グラウンドに接続され、該第1端子からみたインピーダンスZ1が該第2端子からみたインピーダンスZ2に実質的に等しい関係を維持しつつ、該第1端子および該第2端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、該第2状態において、該第1端子は、該第3端子に接続され、該第1端子は、該第2端子から遮断され、該第2端子は、グラウンドに接続され、該第1端子からみたインピーダンスZ1が該第3端子からみたインピーダンスZ3に実質的に等しい関係を維持しつつ、該第1端子および該第3端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、そのことにより上記目的が達成される。

【0013】ある実施形態では、第1トランジスタが、前記第1端子とグラウンドとの間に設けられ、第2トランジスタが、前記第2端子とグラウンドとの間に設けられ、第3トランジスタが、前記第3端子とグラウンドとの間に設けられ、第4トランジスタが、該第1端子と該第2端子との間に設けられ、第5トランジスタが、該第1端子と該第3端子との間に設けられており、前記第1状態において、該第3トランジスタは、オン状態であり、該第5トランジスタは、オフ状態であり、前記第2状態において、該第3トランジスタは、オン状態であり、該第5トランジスタは、オフ状態である。

【0014】ある実施形態では、前記インピーダンスZ1は、0.5×ZA～2.0×ZAの範囲に実質的に含

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まれ、前記インピーダンスZ2は、 $0.5 \times Z_T \sim 2.0 \times Z_T$ の範囲に実質的に含まれ、前記インピーダンスZ3は、 $0.5 \times Z_R \sim 2.0 \times Z_R$ の範囲に実質的に含まれ、ここでZA、ZTおよびZRは、それぞれ前記アンテナ、前記送信機および前記受信機のインピーダンスを表す。

【0015】ある実施形態では、前記第1トランジスタ、前記第2トランジスタ、前記第3トランジスタ、前記第4トランジスタおよび前記第5トランジスタのそれぞれは、ドレインと、ソースと、2つのゲートとを有するデュアルゲート電界効果トランジスタであり、該2つのゲートの一方のゲートは、該ドレインに接続されており、該2つのゲートの他方のゲートは、該ソースに接続されており、該2つのゲートは、それぞれ抵抗を介して電気的な制御のための電圧を受け取る。

【0016】本発明によるスイッチアッテネータは、第1アンテナに接続される第1端子と、送信機に接続される第2端子と、受信機に接続される第3端子と、第2アンテナに接続される第4端子とを備え、第1状態、第2状態、第3状態および第4状態を切り替えるスイッチアッテネータであって、該第1状態においては、該第1端子は、該第2端子に接続され、かつ該第3端子から遮断され、該第3端子は、グラウンドに接続され、該第4端子は、該第1端子、該第2端子、該第3端子および該グラウンドから遮断され、該第1端子からみたインピーダンスZ1が該第2端子からみたインピーダンスZ2に実質的に等しい関係を維持しつつ、該第1端子および該第2端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、該第2状態においては、該第1端子は、該第3端子に接続され、かつ該第2端子から遮断され、該第2端子は、グラウンドに接続され、該第4端子は、該第1端子、該第2端子、該第3端子および該グラウンドから遮断され、該第1端子からみたインピーダンスZ1が該第3端子からみたインピーダンスZ2に実質的に等しい関係を維持しつつ、該第1端子および該第3端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、該第3状態においては、該第4端子は、該第2端子に接続され、かつ該第3端子から遮断され、該第3端子は、グラウンドに接続され、該第1端子は、該第2端子、該第3端子、該第4端子および該グラウンドから遮断され、該第4端子からみたインピーダンスZ4が該第2端子からみたインピーダンスZ2に実質的に等しい関係を維持しつつ、該第4端子および該第2端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、該第4状態においては、該第4端子は、該第3端子に接続され、かつ該第2端子から遮断され、該第2端子は、グラウンドに接続され、該第1端子は、該第2端子、該第3端子、該第4端子および該グラウンドから遮断され、該第4端子からみたインピーダンスZ4が該第3端子からみたインピーダンスZ3に実質的に等しい関係を維持しつつ、該第4端子および該第3端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能である。

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ダンスZ4が該第3端子からみたインピーダンスZ3に実質的に等しい関係を維持しつつ、該第4端子および該第3端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、そのことにより上記目的が達成される。

【0017】ある実施形態では、第1トランジスタが、前記第1端子とグラウンドとの間に設けられ、第2トランジスタが、前記第2端子とグラウンドとの間に設けられ、第3トランジスタが、前記第3端子とグラウンドとの間に設けられ、第4トランジスタが、該第1端子と該第2端子との間に設けられ、第5トランジスタが、該第1端子と該第3端子との間に設けられ、第6トランジスタが、前記第4端子とグラウンドとの間に設けられ、第7トランジスタが、該第2端子と該第4端子との間に設けられ、第8トランジスタが、該第3端子と該第4端子との間に設けられ、前記第1状態において、該第3トランジスタは、オン状態であり、該第5トランジスタ、該第6トランジスタ、該第7トランジスタおよび該第8トランジスタは、オフ状態であり、前記第2状態において、該第2トランジスタは、オン状態であり、該第4トランジスタ、該第6トランジスタ、該第7トランジスタおよび該第8トランジスタは、オフ状態であり、前記第3状態において、該第3トランジスタは、オン状態であり、該第1トランジスタ、該第4トランジスタ、該第5トランジスタおよび該第8トランジスタは、オフ状態であり、前記第4状態において、該第2トランジスタは、オン状態であり、該第1トランジスタ、該第4トランジスタ、該第5トランジスタおよび該第7トランジスタは、オフ状態である。

30 【0018】ある実施形態では、前記インピーダンスZ1およびZ4は、 $0.5 \times Z_A \sim 2.0 \times Z_A$ の範囲に実質的に含まれ、前記インピーダンスZ2は、 $0.5 \times Z_T \sim 2.0 \times Z_T$ の範囲に実質的に含まれ、前記インピーダンスZ3は、 $0.5 \times Z_R \sim 2.0 \times Z_R$ の範囲に実質的に含まれ、ここでZA、ZTおよびZRは、それぞれ前記アンテナ、前記送信機および前記受信機のインピーダンスを表す。

【0019】ある実施形態では、半導体基板上に集積化されて形成されている。

40 【0020】ある実施形態では、電力増幅器をさらに備えており、該電力増幅器は、前記半導体基板上に集積化されて形成されている。

【0021】ある実施形態では、低雑音増幅器をさらに備えており、該低雑音増幅器は、前記半導体基板上に集積化されて形成されている。

[0022]

【発明の実施の形態】以下、本発明の実施の形態を図面を参照しながら説明する。同じ参照符号は、同じ構成要素を表す。

50 【0023】本明細書における「スイッチアッテネー

タ」は、後述するようにアンテナ用RFスイッチとRFアッテネータとの機能を併せもつ装置をいう。また「ノード」は、装置外部への接続のための端子を必ずしも必要としない。

【0024】(実施の形態1) 図3は、本発明のスイッチアッテネータの第1の実施形態が用いられる携帯電話機のRF部30のブロック図である。本発明のスイッチアッテネータ40は、送受信の状態に応じて、アンテナ130と、電力増幅器116または低雑音増幅器152とを電気的に結合する。より具体的には、スイッチアッテネータ40は、送信時にはノードT1をノードT2に電気的に結合し、ノードT3をグラウンドに電気的に結合する。またスイッチアッテネータ40は、受信時にはノードT1をノードT3に電気的に結合し、ノードT2をグラウンドに電気的に結合する。本明細書におけるグラウンドは、電源の負極が接続されており、直流(以下「DC」とする)信号およびRF信号の双方について共通電位を提供するとともに、高周波的にシールドされた筐体などにも接続されている。RF部30における送受信時の信号の流れは、図1で説明したのと同様である。

【0025】本発明によるスイッチアッテネータ40は、後述するように、スイッチおよびアッテネータの機能を併せもつて、図1のAGCアンプ114およびアッテネータ150をなくすことができるという大きな効果を有する。またスイッチアッテネータ40を一体化された半導体デバイスとして製造すれば、サイズおよびコストの大半な削減が可能となりより好ましい。なお図3のそれぞれのブロックを接続する伝送線路は、すべて50Ωの特性インピーダンスを有する。またここではRF部30は、携帯電話機の一部として用いられているが、これには限定されない。RF部30は、RF信号を送受信する装置に広く利用することができ、またスイッチアッテネータ40は、RF信号を切り替えるとともに、減衰させる装置として広く利用できる。

【0026】図3において、制御電圧発生器CV1は、スイッチアッテネータ40に含まれるFETの状態を後で説明する表1～表4のように設定するための制御電圧をリードオンリーメモリROM1に格納されたデータに基づいて発生し、それぞのFETに供給する。リードオンリーメモリROM1は、表1～表4の状態に対応するFETの制御電圧を発生するためのデータを格納する。

【0027】図4は、本発明によるスイッチアッテネータの第1の実施形態の回路図である。スイッチアッテネータ40は、ノードT1、T2およびT3を備えており、それぞれアンテナ130、電力増幅器116および低雑音増幅器152に接続されている。制御電圧発生器CV1は、リードオンリーメモリROM1に格納されたデータに基づいてFETを制御する電圧を発生し、ノードCT1～CT5に出力する。

【0028】FET Q1は、ノードT1をあるインピーダンスでグラウンドに接続する。ノードCT1において受け取られた制御電圧は、抵抗R12を介してFET Q1のゲートに加えられ、FET Q1のこの所定のインピーダンスを変化させる。具体的には、ノードCT1の制御電圧に応じて、FET Q1は、オン状態からオフ状態までの広い範囲のインピーダンスをとりうる。FET Q1のインピーダンスは、オン状態ではゼロであるとみなせる程度に低く、オフ状態では無限大であるとみなせる程度に高い。FET Q1はN型のディプレッション型であるので、FET Q1をオン状態にするためには、0[V]以上のゲート・ソース間電圧Vgsを与えるべく、逆にFET Q1をオフ状態にするためには、閾値VTH[V](VTH<0)以下のゲート・ソース間電圧Vgsを与えるべし。FET Q1のゲート・ソース間電圧Vgsが、VTH<Vgs<0なる関係を満たすとき、本明細書においてはFET Q1は、オン状態とオフ状態との「中間状態」であるとよぶこととする。FET Q1は、本実施の形態では、ショットキー接合ゲート型FET(以下「MESFET」とする)である。以上、FET Q1についての説明は、本明細書において、FET Q2～Q4についてもあてはまる。

【0029】FET Q1と同様に、FET Q2およびQ3は、それぞれノードT2およびT3をあるインピーダンスでグラウンドに接続する。ノードCT2およびCT3において受け取られた制御電圧は、それぞれ、抵抗R22を介してFET Q2のゲートに、また抵抗R32を介してFET Q3のゲートに加えられ、それぞれFET Q2およびQ3のインピーダンスを変化させる。抵抗R12、R22およびR32は、ゲートバイアス用の抵抗である。

【0030】FET Q1、Q2およびQ3のソースとグラウンドとの間には、それぞれ抵抗R11、R21およびR31が設けられている。これらの抵抗R11、R21およびR31は、それぞれFET Q1、Q2およびQ3がオン状態のときのノードT1、T2およびT3とグラウンドとの間のインピーダンスを調整することによって、インピーダンス整合をとる。

【0031】FET Q1と同様に、FET Q4およびQ5は、それぞれノードT2およびT3をあるインピーダンスでノードT1に接続する。ノードCT4およびCT5において受け取られた制御電圧は、それぞれ抵抗R42を介してFET Q4のゲートに、また抵抗R52を介してFET Q5のゲートに加えられ、それぞれFET Q4およびQ5のインピーダンスを変化させる。

【0032】次にスイッチアッテネータ40の動作を説明する。スイッチアッテネータ40は、以下の動作モード1～4を有する。すなわち、

モード1：減衰なしの送信、

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モード2：減衰ありの送信、
モード3：減衰なしの受信、および
モード4：減衰ありの受信

である。ここで「減衰」とは、ノードT1と、ノードT2またはノードT3との間における減衰をいう。例えばモード1においては、ノードT1およびノードT2の間の減衰が存在しない。モード1は、RF部30を含む移動端末機が基地局から離れている場合、つまり電力増幅器116から出力されたRF信号を減衰させることなくアンテナ130に供給する場合に用いられる。モード2は、逆にRF部30を含む移動端末機が基地局に近い場合、つまり電力増幅器116から出力されたRF信号を減衰させてからアンテナ130に供給する場合に用いられる。送信の場合と同様のことが受信の場合にもあてはまる。モード3は、RF部30を含む移動端末機が基地局から離れている場合、つまりアンテナ130から入力されたRF信号を減衰させることなく低雑音増幅器152

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*2に供給する場合に用いられる。モード4は、逆にRF部30を含む移動端末機が基地局に近い場合、つまりアンテナ130から入力されたRF信号を減衰させてから低雑音増幅器152に供給する場合に用いられる。

【0033】本発明のスイッチアッテネータ40は、後述するようにモード2およびモード4において、スイッチング素子（ここではFET）の制御電圧を変化させることによって、スイッチアッテネータ40の減衰量を連続的に変化させることができる。その結果、本発明のスイッチアッテネータは、送信時の出力電力、および受信時の入力電力が広いレンジをとりうる移動通信において大きな効果を奏す。

【0034】（モード1）モード1におけるスイッチアッテネータ40のFET Q1～Q5の状態を表1に示す。

【0035】

【表1】

FET	Q1	Q2	Q3	Q4	Q5
状態	オフ	オフ	オン	オン	オフ

【0036】スイッチアッテネータ40のモード1を実現するためには、FET Q1～Q5を表1に示す状態に設定する、それぞれの状態に対応する制御電圧をノードCT1～CT5に印加すればよい。前述したように、FET Q1～Q5をオン状態にするためには、例えば0[V]以上の電圧をそれぞれのゲートに加えればよく、FET Q1～Q5をオフ状態にするためには、例えばVTH[V]以下の電圧をそれぞれのゲートに加えればよい。

【0037】図5は、モード1におけるスイッチアッテネータ40の等価回路図である。図5において、閉じたスイッチはオン状態のFETを表し、開いたスイッチはオフ状態のFETを表す。モード1においては図5に示すように、ノードT1はほぼインピーダンスがゼロでノードT2に接続され、ノードT3はほぼインピーダンスがゼロでグラウンドに接続され、ノードT3は、ノードT1およびノードT2から遮断されている。したがって※

※モード1においては、電力増幅器116から出力されたRF信号は、ノードT2において受け取られ、減衰されることなくFET Q4およびノードT1を通ってアンテナ130に供給される。また低雑音増幅器152への入力端子であるノードT3は、FET Q3によってグラウンドに接続され、それにより不要なRF信号が低雑音増幅器152へ入力されることを防ぐ。

【0038】モード1におけるスイッチアッテネータ40の挿入損失は、FET Q4のオン状態のインピーダンス（つまりオン抵抗に相当するインピーダンス）に起因する約0.5dBだけである。

【0039】（モード2）モード2におけるスイッチアッテネータ40のFET Q1～Q5の状態を表2に示す。

【0040】

【表2】

FET	Q1	Q2	Q3	Q4	Q5
状態	中間	中間	オン	中間	オフ

【0041】スイッチアッテネータ40のモード2を実現するためには、FET Q1～Q5を表2に示す状態に設定する、それぞれの状態に対応する制御電圧をノードCT1～CT5に印加すればよい。モード2およびモード4においては、FETを中間状態で用いる。FET Q1～Q5を中間状態にするためには、ゲート・ソース間電圧Vgsとして、 $0 < V_{gs} < V_{TH}$ なる電圧をそれぞれのゲートに加えればよい。

【0042】図6は、モード2におけるスイッチアッテ

ネータ40の等価回路図である。図6において、閉じたスイッチはオン状態のFETを表し、開いたスイッチはオフ状態のFETを表し、抵抗は中間状態のFETを表す。以下、中間状態のFET Q1～Q5のインピーダンスを、それぞれZQ1～ZQ5のように表すこととする。モード2においては図6に示すように、ノードT1はインピーダンスZQ4でノードT2に接続され、インピーダンスZQ1でグラウンドに接続される。ノードT2はインピーダンスZQ2でグラウンドに接続される。

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ノードT3はほぼインピーダンスがゼロでグラウンドに接続され、かつノードT3は、ノードT1およびノードT2から遮断されている。したがってモード2においては、電力増幅器116から出力されたRF信号は、ノードT2において受け取られ、所望の減衰量を伴ってFET Q1、Q2およびQ4およびノードT1を通ってアンテナ130に供給される。また低雑音増幅器152への入力端子であるノードT3は、FET Q3によってグラウンドに接続され、それにより不要なRF信号が低雑音増幅器152へ入力されることを防ぐ。

【0043】モード2におけるスイッチアッテネータ40の減衰量は、FET Q1、Q2およびQ4のゲートに加えられる制御電圧を変化させること、すなわちインピーダンスZQ1、ZQ2およびZQ4を変化させることによって変わる。FET Q1、Q2およびQ4のゲートに加えられる制御電圧の値は、例えばあらかじめリードオンリーメモリROM1に格納されており、必要な減衰量

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* 衰量に応じて読み出される。例えばプログラマブルな電圧発生器である制御電圧発生器CV1がROM1から読み出された制御電圧を表すデータに基づいて制御電圧を発生し、それぞれのFETのゲートに出力すれば、所望の量だけRF信号を減衰させるためのモード2およびモード4を実現できる。またROM1は、FET Q3およびQ5のゲートに加えられる制御電圧(つまりそれぞれ0[V]以上の電圧およびVTH[V]以下の電圧)を表すデータを併せて格納してもよい。さらにROM1は、モード1、3および4においてFET Q1～Q5に加えられる制御電圧を表すデータを併せて格納してもよい。

【0044】(モード3) モード3におけるスイッチアッテネータ40のFET Q1～Q5の状態を表3に示す。

【0045】

【表3】

FET	Q1	Q2	Q3	Q4	Q5
状態	オフ	オン	オフ	オフ	オン

【0046】スイッチアッテネータ40のモード3を実現するためには、FET Q1～Q5を表3に示す状態に設定する、それぞれの状態に対応する制御電圧をノードCT1～CT5に印加すればよい。

【0047】図7は、モード3におけるスイッチアッテネータ40の等価回路図である。モード3においては図7に示すように、ノードT1はほぼインピーダンスがゼロでノードT3に接続され、ノードT2はほぼインピーダンスがゼロでグラウンドに接続され、ノードT2は、ノードT1およびノードT3から遮断されている。したがってモード3においては、アンテナ130から入力されたRF信号は、ノードT1において受け取られ、減衰されることなくFET Q5およびノードT3を通って※

※ 低雑音増幅器152に供給される。また電力増幅器116からの出力端子であるノードT2は、FET Q2によってグラウンドに接続され、それにより不要なRF信号が低雑音増幅器152へ出力されることを防ぐ。

【0048】モード3におけるスイッチアッテネータ40の挿入損失は、FET Q5のオン状態のインピーダンスに起因する約0.5dBだけである。

【0049】(モード4) モード4におけるスイッチアッテネータ40のFET Q1～Q5の状態を表4に示す。

【0050】

【表4】

FET	Q1	Q2	Q3	Q4	Q5
状態	中間	オン	中間	オフ	中間

【0051】スイッチアッテネータ40のモード4を実現するためには、FET Q1～Q5を表4に示す状態に設定する、それぞれの状態に対応する制御電圧をノードCT1～CT5に印加すればよい。

【0052】図8は、モード4におけるスイッチアッテネータ40の等価回路図である。モード4においては図8に示すように、ノードT1はインピーダンスZQ5でノードT3に接続され、インピーダンスZQ1でグラウンドに接続される。ノードT3はインピーダンスZQ3でグラウンドに接続される。ノードT2はほぼインピーダンスがゼロでグラウンドに接続され、かつノードT2は、ノードT1およびノードT3から遮断されている。したがってモード4においては、アンテナ130から入力されたRF信号は、ノードT1において受け取られ、

所望の減衰量を伴ってFET Q1、Q3およびQ5およびノードT3を通って低雑音増幅器152に供給される。また電力増幅器116からの出力端子であるノードT2は、FET Q2によってグラウンドに接続され、それにより不要なRF信号が低雑音増幅器152へ入力されることを防ぐ。

【0053】モード4におけるスイッチアッテネータ40の減衰量は、FET Q1、Q3およびQ5のゲートに加えられる制御電圧を変化させること、すなわちインピーダンスZQ1、ZQ3およびZQ5を変化させることによって変わる。FET Q1、Q3およびQ5のゲートに加えられる制御電圧の値は、モード2で説明したように例えばあらかじめリードオンリーメモリROM1に格納されており、必要な減衰量に応じて読み出される。

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【0054】第1の実施の形態によればモード2において、実質的に $Z_{T1} = Z_{T2} = Z_0$ なる関係を満たしたままで減衰量を変化させることができる。ここでインピーダンス Z_{T1} は、ノードT1から見たスイッチアッテネータ40のインピーダンスを表し、インピーダンス Z_{T2} は、ノードT2から見たスイッチアッテネータ40のインピーダンスを表し、インピーダンス Z_0 は、外部に接続された回路の特性インピーダンス（例えば 50Ω ）を表す。同様に第1の実施の形態によればモード4において、実質的に $Z_{T1} = Z_{T3} = Z_0$ なる関係を満たしたままで減衰量を変化させることができる。ここでインピーダンス Z_{T3} は、ノードT3から見たスイッチアッテネータ40のインピーダンスを表す。

【0055】また上記 $Z_{T1} = Z_{T2} = Z_0$ および $Z_{T1} = Z_{T3} = Z_0$ なる関係が満たされなくとも、

$$\begin{aligned} 0.5 \times Z_A &\leq Z_{T1} \leq 2.0 \times Z_A, \\ 0.5 \times Z_T &\leq Z_{T2} \leq 2.0 \times Z_T, \text{ および} \\ 0.5 \times Z_R &\leq Z_{T3} \leq 2.0 \times Z_R, \end{aligned}$$

という関係が満たされることが好ましい。ここでインピーダンス Z_A は、ノードT1に接続される回路（ここではアンテナ130）の特性インピーダンスを表し、インピーダンス Z_T は、ノードT2に接続される回路（ここでは電力増幅器116）の特性インピーダンスを表し、インピーダンス Z_R は、ノードT3に接続される回路（ここでは低雑音増幅器152）の特性インピーダンスを表す。

【0056】図9は、半導体基板上に集積化して形成された本発明のスイッチアッテネータ40の平面図である。図9に示すようにスイッチアッテネータ40は、ガリウムヒ素（以下「GaAs」とする）基板901上に集積化されて形成されている。図9の「GND」は、グラウンドを表し、他の参照符号は図4のなかのそれらと対応する。FET Q1～Q5はMOSFETであり、GaAs基板901上にイオン注入法により形成される。FET Q1～Q5のサイズは、ゲート長が $0.5 \mu\text{m}$ であり、ゲート幅が $800 \mu\text{m}$ である。図9に示すスイッチアッテネータ40を実現した半導体チップは、10ピンの樹脂モールドパッケージに封止されて供用される。

【0057】（実施の形態2）図10は、本発明によるスイッチアッテネータの第2の実施形態の回路図である。図10のFET Q1D、Q2D、Q3D、Q4DおよびQ5Dは、デュアルゲートFETである。FET

Q1D～Q5Dの第1ゲートおよび第2ゲートには、それぞれゲートバイアス抵抗器R13およびR14と、R23およびR24と、R33およびR34と、R43およびR44と、R53およびR54とが接続されている。またFET Q1D～Q5Dの第2ゲートとドレンとの間には、それぞれコンデンサC13、C23、C33、C43およびC53が接続されており、FET

Q1D～Q5Dの第1ゲートとソースとの間には、それぞれコンデンサC14、C24、C34、C44およびC54が接続されている。

【0058】第2の実施形態は、シングルゲートFETの代わりにデュアルゲートFETが用いられていることと、ドレンと第2ゲートとの間、およびソースと第1ゲートとの間にコンデンサが接続されていることが第1の実施形態と異なる。第2の実施形態の構成によれば、FETのもつ非線形性を低減することができ、優れた歪特性を実現できる。

【0059】（実施の形態3）図11は、本発明のスイッチアッテネータの第3の実施形態が用いられる携帯電話機のRF部1100のブロック図である。本発明のスイッチアッテネータ1200は、送受信の状態に応じて、アンテナ130または131と、電力増幅器116または低雑音増幅器152とを電気的に結合する。

【0060】より具体的には、スイッチアッテネータ1200は、送信時にはノードT1およびT4のうちの1つをノードT2に電気的に結合し、ノードT3をグラウンドに電気的に結合し、ノードT1およびT4のうちノードT2に結合されていないノードを他のノードおよびグラウンドから遮断する。

【0061】またスイッチアッテネータ1200は、受信時にはノードT1およびT4のうちの1つをノードT3に電気的に結合し、ノードT2をグラウンドに電気的に結合し、ノードT1およびT4のうちノードT3に結合されていないノードを他のノードおよびグラウンドから遮断する。第3の実施形態は、第1の実施形態が単一のアンテナを用いたのと異なり、2つのアンテナ130および131を利用することができる。したがって第3の実施形態は、第1の実施形態の効果に加えて、2つのアンテナ130および131を送受信の状況に応じて選択的に利用できるという効果を有する。この第3の実施形態の構成は、例えば空間ダイバーシティ送受信を可能にする。なお図11のそれぞれのブロックを接続する伝送線路は、すべて 50Ω の特性インピーダンスを有する。

【0062】図11および図12における制御電圧発生器CV2およびリードオンリーメモリROM2は、FETを制御する電圧を供給するノードがCT1～CT8であることを除いて、制御電圧発生器CV1およびリードオンリーメモリROM1と同様に機能する。

【0063】図12は、本発明によるスイッチアッテネータの第3の実施形態の回路図である。スイッチアッテネータ1200は、ノードT4を、ノードT2およびT3のうちの1つに電気的に結合するために、スイッチアッテネータ40の構成要素に加えて、FET Q6～Q8と、ゲートバイアス用の抵抗R62、R72およびR82と、ノードCT6～CT8と、インピーダンス整合用の抵抗R61とをさらに備えている。

【0064】次にスイッチアッテネータ1200の動作

を説明する。スイッチアッテネータ1200は、以下の動作モード1～8を有する。すなわち、

モード1：アンテナ130を用いた減衰なしの送信、
モード2：アンテナ130を用いた減衰ありの送信、
モード3：アンテナ130を用いた減衰なしの受信、
モード4：アンテナ130を用いた減衰ありの受信、
モード5：アンテナ131を用いた減衰なしの送信、
モード6：アンテナ131を用いた減衰ありの送信、
モード7：アンテナ131を用いた減衰なしの受信、および

モード8：アンテナ131を用いた減衰ありの受信である。第3の実施形態のモード1～4は、第1の実施形態のモード1～モード4にそれぞれ対応する。第3の*

*実施形態のモード5～8は、ノードT1の代わりにノードT4がノードT2またはT3に電気的に結合されることを除き、モード1～4と同じである。

【0065】スイッチアッテネータ1200のモード1～8を実現するためには、FET Q1～Q8をそれぞれ以下表5～表12に示す状態に設定する、それぞれの状態に対応する制御電圧をノードCT1～CT8に印加すればよい。スイッチアッテネータ1200のモード1～モード8の等価回路図をそれぞれ図13～図20に示す。

10 【0066】

【表5】

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オフ	オン	オン	オフ	オフ	オフ	オフ

【0067】

※ ※ 【表6】

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	中間	中間	オン	中間	オフ	オフ	オフ	オフ

【0068】

★ ★ 【表7】

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オン	オフ	オフ	オン	オフ	オフ	オフ

【0069】

☆ ☆ 【表8】

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	中間	オン	中間	オフ	中間	オフ	オフ	オフ

【0070】

◆ ◆ 【表9】

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オフ	オン	オフ	オフ	オフ	オン	オフ

【0071】

* * 【表10】

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	中間	オン	オフ	オフ	中間	中間	オフ

【0072】

※ ※ 【表11】

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オン	オフ	オフ	オフ	オフ	オフ	オン

【0073】

★ ★ 【表12】

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オン	中間	オフ	オフ	中間	オフ	中間

【0074】第3の実施の形態では、第1の実施の形態と同様に、モード2および4において、それぞれ実質的にZT1=ZT2=Z0およびZT1=ZT3=Z0なる関係を満たしたままで減衰量を変化させることができ。ここでインピーダンスZT4は、ノードT4から見たスイッチアッテネータ1200のインピーダンスを表す。

T4 = ZT3 = Z0なる関係を満たしたままで減衰量を変化させることができる。ここでインピーダンスZT4は、ノードT4から見たスイッチアッテネータ1200のインピーダンスを表す。

【0075】また上記ZT1=ZT2=Z0、ZT1=ZT3=Z0、ZT4=ZT2=Z0およびZT4=Z

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$T_3 = Z_0$ なる関係が満たされなくとも、
 $0.5 \times Z_A \leq Z_T 1 \leq 2.0 \times Z_A$ 、
 $0.5 \times Z_T \leq Z_T 2 \leq 2.0 \times Z_T$ 、
 $0.5 \times Z_R \leq Z_T 3 \leq 2.0 \times Z_R$ 、および
 $0.5 \times Z_B \leq Z_T 4 \leq 2.0 \times Z_B$

という関係が満たされることが好ましい。ここでインピーダンス Z_B は、ノード T_4 に接続される回路（ここではアンテナ 131 ）の特性インピーダンスを表す。

【0076】以上説明した第1～第3の実施の形態では、FETをオンおよびオフの中間の状態に設定することにより、スイッチアッテネータに接続される回路の特性が変化した場合にも柔軟に対応することができる。このような接続される回路の特性変化は、例えば送信用の電力増幅器から出力される電力を変化させたときなどに起こりうる。

【0077】上記実施の形態では、例えば携帯電話機と基地局との間の通信で用いられる周波数帯において所望の特性インピーダンスが得られるが、この周波数帯には限定されず、広くRF帯に適用できる。

【0078】第2の実施の形態の開示に基づいて、第3の実施の形態のFETをデュアルゲートFETに置き換えることによって、優れた歪特性が実現できるというさらなる効果を得ることもできる。

【0079】本発明のスイッチアッテネータに用いられるFETは、ディブレッション型に限定されず、エンハンスマント型を用いてもよい。またFETは、上記実施形態ではMESFETであるがこれには限定されず、その制御端子によって電気的にインピーダンスを制御できるデバイスであればよい。使用周波数、およびデバイス固有の寄生容量などの条件が許すのであれば、例えばPINダイオード、PN接合型FET、MOS型FETなどを用いてもよい。

【0080】また本発明によるスイッチアッテネータを電力増幅器または低雑音増幅器とともに半導体基板上に集積化して形成すれば、サイズおよびコストの低減を図ることができ、より好ましい。

【0081】制御電圧発生器 CV_1 および CV_2 と、リードオンリーメモリ ROM_1 および ROM_2 とは、本発明によるスイッチアッテネータのFETの状態をオン状態、中間状態およびオフ状態のいずれかの状態に設定するための制御電圧を発生できるのであれば、上記実施の形態で説明された構成には限られない。例えばデータをディジタル的に格納するメモリをもたない、プログラマブルな電圧発生器を用いてもよい。またリードオンリーメモリ ROM_1 および ROM_2 の代わりに、ランダムアクセスメモリを用いてもよい。

【0082】表2、表4、表6、表8、表10および表12に示すように、上述の実施の形態では、減衰ありの送信または受信時には、3個のFETを中間状態に設定している。しかし中間状態のFETの個数は、3個に限

られず、少なくとも1個のFETが中間状態であることによって所望の減衰量が得られればよい。

【0083】

【発明の効果】以上のように本発明によれば、高周波機器において、送信と受信の切り替えや複数のアンテナの切り替えと同時に減衰量を自由に制御することが、一つの半導体素子で実現でき、機器の小型軽量化や低コスト化が図れるという顕著な効果が得られる。

【図面の簡単な説明】

【図1】従来の技術による送受信回路の高周波部10のブロック図である。

【図2】従来の技術によるスイッチ20の回路図である。

【図3】本発明のスイッチアッテネータの第1の実施形態が用いられる携帯電話機のRF部30のブロック図である。

【図4】本発明によるスイッチアッテネータの第1の実施形態の回路図である。

【図5】モード1におけるスイッチアッテネータ40の等価回路図である。

【図6】モード2におけるスイッチアッテネータ40の等価回路図である。

【図7】モード3におけるスイッチアッテネータ40の等価回路図である。

【図8】モード4におけるスイッチアッテネータ40の等価回路図である。

【図9】半導体基板上に集積化して形成された本発明のスイッチアッテネータ40の平面図である。

【図10】本発明によるスイッチアッテネータの第2の実施形態の回路図である。

【図11】本発明のスイッチアッテネータの第3の実施形態が用いられる携帯電話機のRF部1100のブロック図である。

【図12】本発明によるスイッチアッテネータの第3の実施形態の回路図である。

【図13】モード1におけるスイッチアッテネータ1200の等価回路図である。

【図14】モード2におけるスイッチアッテネータ1200の等価回路図である。

【図15】モード3におけるスイッチアッテネータ1200の等価回路図である。

【図16】モード4におけるスイッチアッテネータ1200の等価回路図である。

【図17】モード5におけるスイッチアッテネータ1200の等価回路図である。

【図18】モード6におけるスイッチアッテネータ1200の等価回路図である。

【図19】モード7におけるスイッチアッテネータ1200の等価回路図である。

【図20】モード8におけるスイッチアッテネータ1200

00の等価回路図である。

【符号の説明】

40 スイッチアッテネータ

Q1、Q2、Q3、Q4、Q5 FET

R11、R12、R21、R22、R31、R32、R*

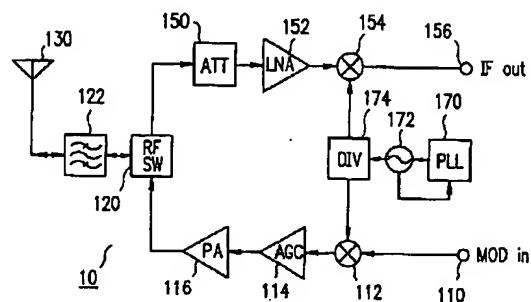
*42、R52 抵抗

T1、T2、T3、CT1、CT2、CT3、CT4、

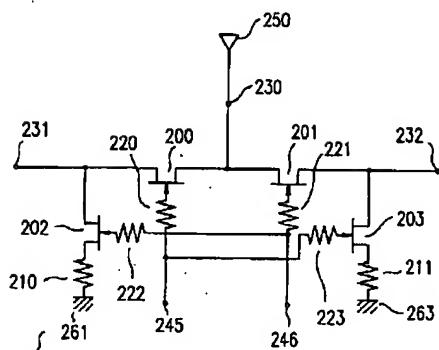
CT5 ノード

130 アンテナ

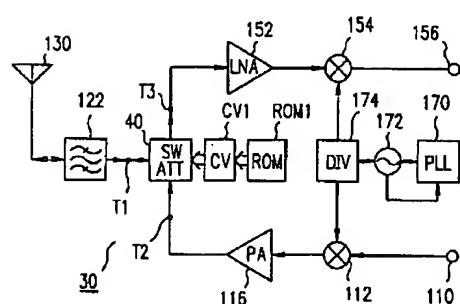
【図1】



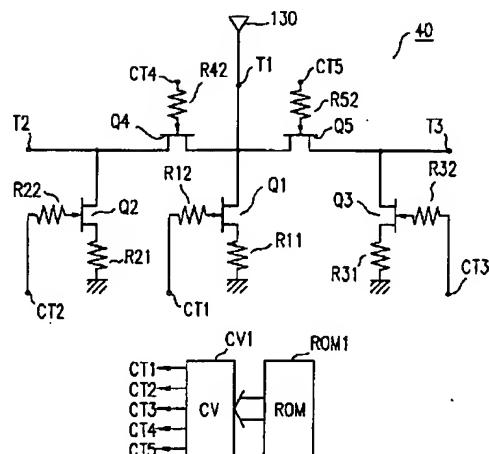
【図2】



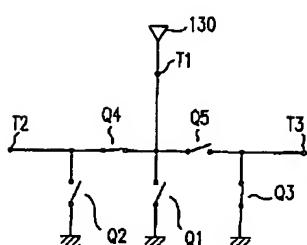
【図3】



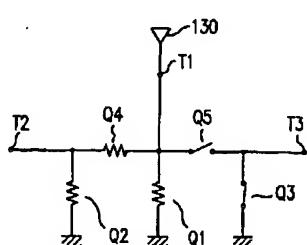
【図4】



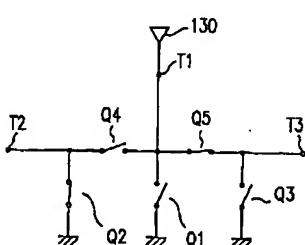
【図5】



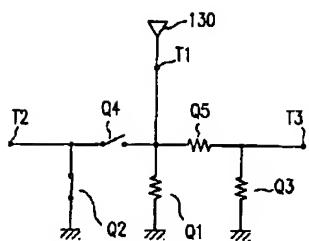
【図6】



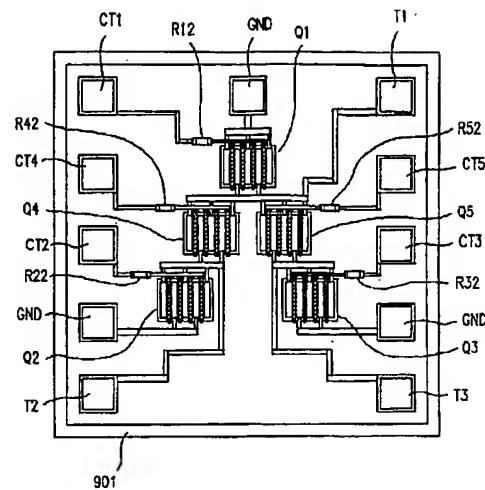
【図7】



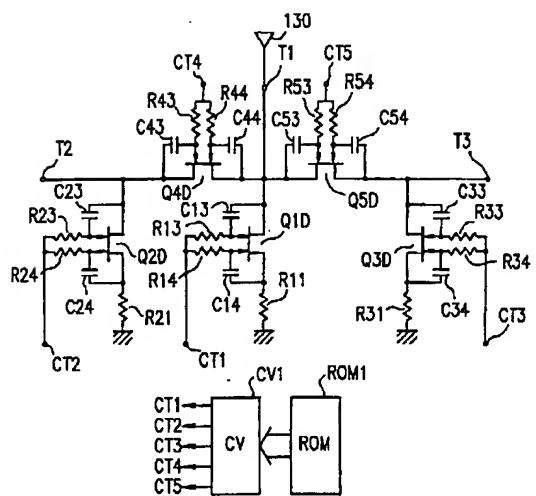
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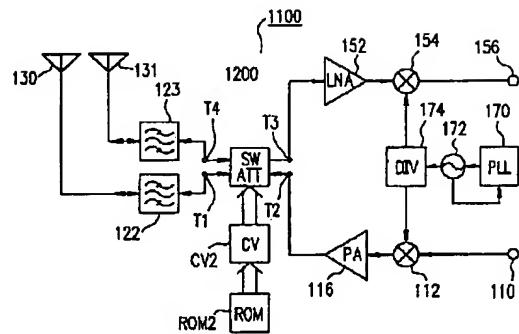
【図9】



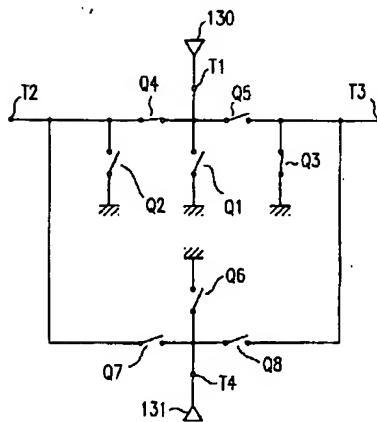
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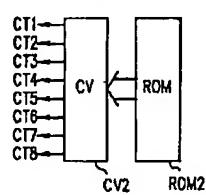
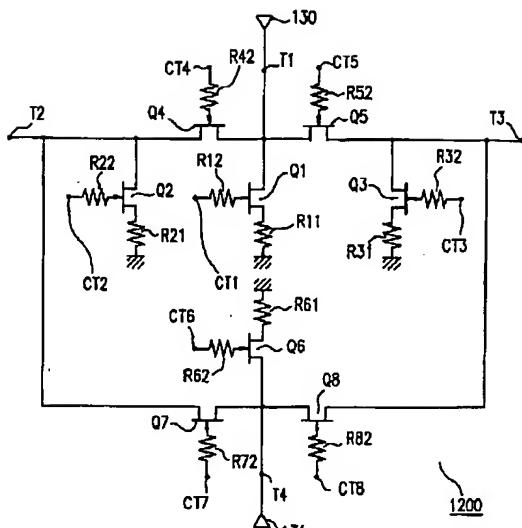
【図11】



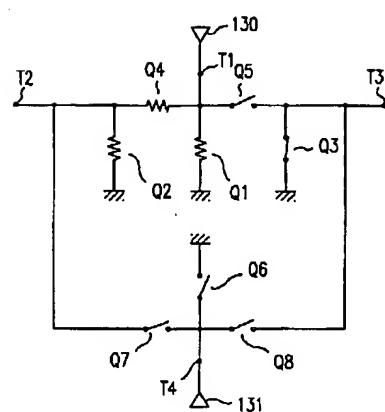
【図13】



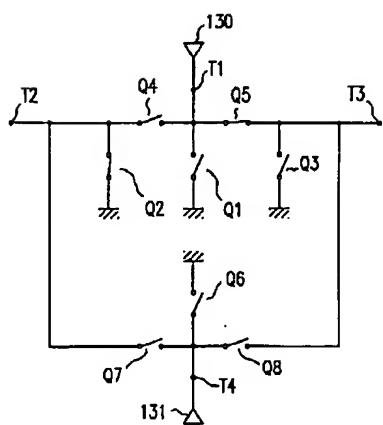
【図12】



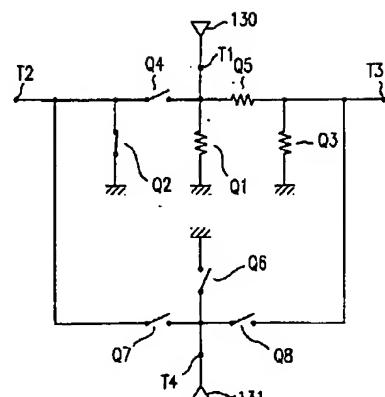
[図14]



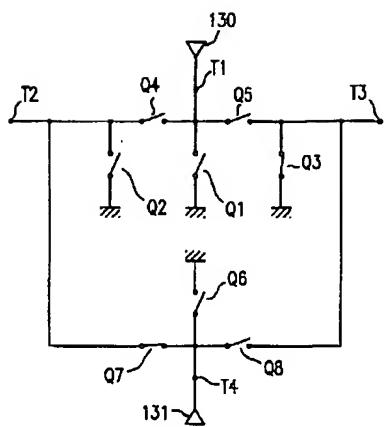
〔图15〕



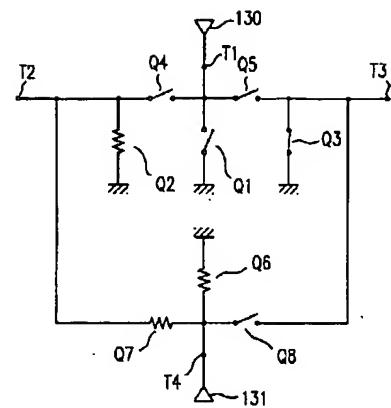
[図16]



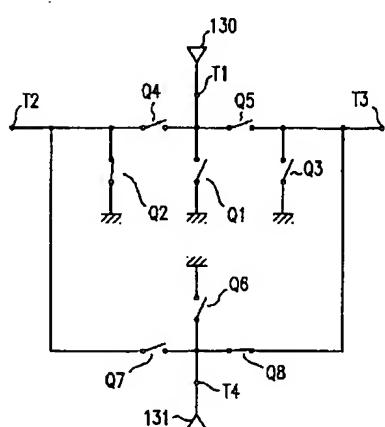
【図17】



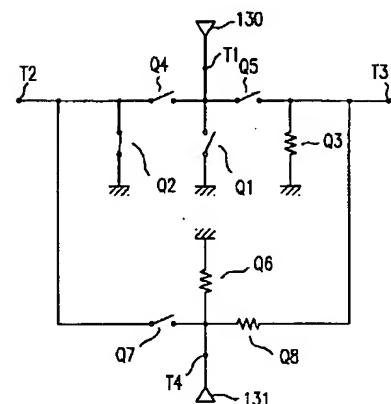
【図18】



【図19】



【図20】



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CLAIMS

[Claim(s)]

[Claim 1] Have the 1st terminal connected to an antenna, the 2nd terminal connected to a transmitter, and the 3rd terminal connected to a receiver, and are the switch attenuator which changes the 1st condition and the 2nd condition, and it sets in this 1st condition. This 1st terminal is connected to this 2nd terminal. This 1st terminal The impedance Z1 which it was intercepted from this 3rd terminal, and this 3rd terminal was connected to the ground, and was seen from this 1st terminal maintaining equal relation substantially to the impedance Z2 seen from this 2nd terminal This switch attenuator is electrically controllable and it sets in this 2nd condition so that the magnitude of attenuation between this 1st terminal and this 2nd terminal may be changed. This 1st terminal It connects with this 3rd terminal and this 1st terminal is intercepted from this 2nd terminal. This 2nd terminal So that it connects with a ground, and the magnitude of attenuation between this 1st terminal and this 3rd terminal may be changed, the impedance Z1 seen from this 1st terminal maintaining equal relation substantially to the impedance Z3 seen from this 3rd terminal This switch attenuator is a controllable switch attenuator electrically.

[Claim 2] The 1st transistor is prepared between said 1st terminal and grounds. The 2nd transistor is prepared between said 2nd terminal and grounds. The 3rd transistor is prepared between said 3rd terminal and grounds. The 4th transistor is prepared between this 1st terminal and this 2nd terminal, the 5th transistor is prepared between this 1st terminal and this 3rd terminal, and it sets in said 1st condition. It is the switch attenuator according to claim 1 this whose 5th transistor this 3rd transistor is an ON state and is an OFF state, this whose 3rd transistor is an ON state in said 2nd condition and this whose 5th transistor is an OFF state.

[Claim 3] Said impedance Z1 is a switch attenuator according to claim 1 to which it is substantially contained in in the range of 0.5xZA-2.0xZA, and said impedance Z2 is substantially contained in in the range of 0.5xZT-2.0xZT, said impedance Z3 is substantially contained in in the range of 0.5xZR-2.0xZR, and ZA, ZT, and ZR express the impedance of said antenna, said transmitter, and said receiver here, respectively.

[Claim 4] Each of said 1st transistor, said 2nd transistor, said 3rd transistor, said 4th transistor, and said 5th transistor the dual gate field-effect transistor which has a drain, the source, and the two gates -- it is -- this -- one gate of the two gates it connects with this drain -- having -- **** -- this -- the gate of another side of the two gates is connected to this source -- having -- **** -- this -- the switch attenuator according to claim 3 from which the two gates receive the electrical potential difference for electric control through resistance, respectively.

[Claim 5] The 1st terminal connected to the 1st antenna, and the 2nd terminal connected to a transmitter, It has the 3rd terminal connected to a receiver, and the 4th terminal connected to the 2nd antenna. Are the switch attenuator which changes the 1st condition, the 2nd condition, the 3rd condition, and the 4th condition, and it sets in this 1st condition. It connects with this 2nd terminal, and this 1st terminal is intercepted from this 3rd terminal. This 3rd terminal Connect with a ground and this 4th terminal is intercepted from this 1st terminal, this 2nd terminal, this 3rd terminal, and this ground. The impedance Z1 seen from this 1st terminal maintaining equal relation substantially to the impedance Z2 seen from this 2nd terminal, so that the magnitude of attenuation between this 1st terminal and this 2nd terminal may be changed This switch attenuator is electrically controllable and it sets in this 2nd condition. It connects with this 3rd terminal, and this 1st terminal is intercepted from this 2nd terminal. This 2nd terminal Connect with a ground and this 4th terminal is intercepted from this 1st terminal, this 2nd terminal, this 3rd terminal, and this ground. The impedance Z1 seen from this 1st terminal maintaining equal relation substantially to the impedance Z3 seen from this 3rd terminal, so that the magnitude of attenuation between this 1st terminal and this 3rd terminal may be changed This switch attenuator is electrically controllable and it sets in this 3rd condition. It connects with this 2nd terminal, and this 4th terminal is intercepted from this 3rd terminal. This 3rd terminal Connect with a ground and this 1st terminal is intercepted from this 2nd terminal, this 3rd terminal, this 4th terminal, and this

ground. The impedance Z4 seen from this 4th terminal maintaining equal relation substantially to the impedance Z2 seen from this 2nd terminal, so that the magnitude of attenuation between this 4th terminal and this 2nd terminal may be changed. This switch attenuator is electrically controllable and it sets in this 4th condition. It connects with this 3rd terminal, and this 4th terminal is intercepted from this 2nd terminal. This 2nd terminal connects with a ground and this 1st terminal is intercepted from this 2nd terminal, this 3rd terminal, this 4th terminal, and this ground. This switch attenuator is a controllable switch attenuator electrically so that the magnitude of attenuation between this 4th terminal and this 3rd terminal may be changed the impedance Z4 seen from this 4th terminal maintaining equal relation substantially to the impedance Z3 seen from this 3rd terminal.

[Claim 6] The 1st transistor is prepared between said 1st terminal and grounds. The 2nd transistor is prepared between said 2nd terminal and grounds. The 3rd transistor is prepared between said 3rd terminal and grounds. The 4th transistor is prepared between this 1st terminal and this 2nd terminal. The 5th transistor It is prepared between this 1st terminal and this 3rd terminal, and the 6th transistor is prepared between said 4th terminal and grounds. The 7th transistor is prepared between this 2nd terminal and this 4th terminal, the 8th transistor is prepared between this 3rd terminal and this 4th terminal, and it sets in said 1st condition. This 3rd transistor is an ON state. This 5th transistor, this 6th transistor, this 7th transistor, and this 8th transistor It is an OFF state and sets in said 2nd condition. This 2nd transistor It is an ON state. This 4th transistor, this 6th transistor, this 7th transistor, and this 8th transistor It is an OFF state and sets in said 3rd condition. This 3rd transistor It is an ON state. This 1st transistor, this 4th transistor, this 5th transistor, and this 8th transistor It is the switch attenuator according to claim 5 this whose 2nd transistor are an OFF state and is an ON state in said 4th condition and this 1st transistor, this 4th transistor, this 5th transistor, and this whose 7th transistor are OFF states.

[Claim 7] Said impedances Z1 and Z4 are substantially contained in the range of $0.5 \times ZA - 2.0 \times ZA$. Said impedance Z2 It is substantially contained in the range of $0.5 \times ZT - 2.0 \times ZT$. Said impedance Z3 It is the switch attenuator according to claim 5 to which it is substantially contained in the range of $0.5 \times ZR - 2.0 \times ZR$, and ZA, ZT, and ZR express the impedance of said antenna, said transmitter, and said receiver here, respectively.

[Claim 8] A switch attenuator given in either of claim 1 to claims 7 which are integrated and are formed on the semi-conductor substrate.

[Claim 9] It is the switch attenuator according to claim 8 which is further equipped with power amplifier, and this power amplifier is integrated on said semi-conductor substrate, and is formed.

[Claim 10] It is the switch attenuator according to claim 9 which is further equipped with the low noise amplifier, and this low noise amplifier is integrated on said semi-conductor substrate, and is formed.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the switch attenuator containing the high frequency switch and high frequency attenuator which are used for a high frequency transceiver circuit. Moreover, this invention relates to the semiconductor device which realizes this switch attenuator, and the RF device using this semiconductor device.

[0002]

[Description of the Prior Art] Drawing 1 is the block diagram showing the high frequency (referred to as "RF" below) section 10 of the transceiver circuit by the Prior art. The RF section 10 of a transceiver circuit is equipped with the RF switch 120, and, thereby, performs transmission and reception alternatively. At the time of transmission, the signal inputted in the modulating-signal input terminal (MOD in) 110 is radiated from an antenna 130 in space through a frequency converter (it considers as a "mixer" below) 112, a variable gain amplifier (it considers as "AGC amplifier" below) 114, power amplifier (PA) 116, the RF switch (RF SW) 120, and the frequency filter 122.

[0003] Conversely, at the time of reception, the signal received in the antenna 130 is outputted through the frequency filter 122, the RF switch 120, an attenuator 150, a low noise amplifier (LNA) 152, and a mixer 154 from the intermediate frequency (referred to as "IF" below) signal output terminal (IF out) 156.

[0004] transmission and reception -- in any case, a local oscillation signal with a desired frequency is generated, and a phase locked loop (referred to as "PLL" below) 170 and an oscillator 172 output it to a signal distribution box (DIV) 174. By mixing a modulating signal and a local oscillation signal, a mixer 112 generates a RF signal and outputs it to the AGC amplifier 114. By mixing a RF signal and a local oscillation signal, a mixer 154 generates an IF signal and outputs it to the IF signal output terminal 156.

[0005] Actuation of the RF section 10 of drawing 1 is explained below. The RF sections 10 are some mobile transmitters represented by the terminal of a cellular phone. In almost all cases, in a mobile transmitter, the antenna 130 (here, it thinks also including the frequency filter 122) which requires the comparatively big volume for simplification of configuration is used for the both sides of a sending circuit and a receiving circuit. In order to share the antenna section by transmission and reception, at the time of transmission, it is electrically combined with power amplifier 116, and an antenna 130 is electrically separated from a low noise amplifier 152. Conversely, at the time of reception, it dissociates from power amplifier 116 electrically, and an antenna 130 is electrically combined with a low noise amplifier 152. In order to perform the change for such transmission and reception, the semiconductor-device-ized RF switch 120 is usually adopted. The RF switch 120 by the conventional technique uses the transistor as a switching element, and it is controlling it electrically so that a transistor takes the condition of either an ON state and an OFF state.

[0006] Moreover, the terminal (for example, the hand set of a cellular phone itself) in mobile communications transmits a RF signal to a nearby base station, and communicates by receiving a RF signal from a base station. in order to maintain the power received in a base station to about 1 law, according to the distance of a terminal and a base station, it is necessary to control delicately the power transmitted from a terminal In order to maintain almost uniformly the power outputted in the IF signal output terminal 156 of a terminal on the contrary, it is necessary to control RF power inputted into a low noise amplifier 152. In order to fill these demands, generally the RF section 10 of a terminal is equipped with the AGC amplifier 114 for transmission, and the attenuator 150 for reception.

[0007] Drawing 2 is the circuit diagram of the switch 20 by the Prior art. The switch 20 is equipped with field-effect transistors (referred to as "FET" below) 200-203, the resistors 210 and 211 for impedance adjustment, the gate bias resistors 220-223, the antenna terminal 230, the transmitted power-input terminal 231, the received-power output terminal 232, the 1st control terminal 245, and the 2nd control terminal 246 in drawing 2.

[0008] Actuation of the switch of drawing 2 is explained. At the time of transmission, by impressing a negative larger electrical potential difference than the absolute value of the threshold of FET 201 and 202 to the 2nd control terminal 246, FET 201 and 202 is made into an OFF state, and zero or a forward electrical potential difference is impressed to the 1st control terminal 245, and FET 200 and 203 is made into an ON state. Thereby, transmitted power passes along a terminal 231, FET200, and the antenna terminal 230, and is outputted to an antenna 250.

[0009] Conversely, at the time of reception, by impressing a negative larger electrical potential difference than the absolute value of the threshold of FET 200 and 203 to the 1st control terminal 245, FET 200 and 203 is made into an OFF state, and zero or a forward electrical potential difference is impressed to the 2nd control terminal 246, and FET 201 and 202 is made into an ON state. Thereby, received power passes along an antenna 250, a terminal 230, and FET201, and is outputted to a terminal 232.

[0010]

[Problem(s) to be Solved by the Invention] In the migration terminal equipment of a cellular phone, in order to raise portability, while lightweight[small and]-izing a device, low-cost-izing is important. In order to realize this, the miniaturization and low-cost-izing of a circuit in current and the RF section are called for strongly. However, also in which the above-mentioned conventional technique, the transceiver circuit needed to have a switch, AGC amplifier, and an attenuator separately. Consequently, it had the technical problem that the transceiver circuit by the Prior art had the size of a device, and unescapable increase of cost.

[0011] The place which it is made in order that this invention may solve the above-mentioned technical problem, and is made into the purpose is to offer the equipment which functions as small [which is used for a high frequency transceiver circuit], a light and low cost switch, and an attenuator.

[0012]

[Means for Solving the Problem] The 1st terminal by which the switch attenuator by this invention is connected to an antenna, Have the 2nd terminal connected to a transmitter, and the 3rd terminal connected to a receiver, and are the switch attenuator which changes the 1st condition and the 2nd condition, and it sets in this 1st condition. This 1st terminal is connected to this 2nd terminal. This 1st terminal The impedance Z1 which it was intercepted from this 3rd terminal, and this 3rd terminal was connected to the ground, and was seen from this 1st terminal maintaining equal relation substantially to the impedance Z2 seen from this 2nd terminal This switch attenuator is electrically controllable and it sets in this 2nd condition so that the magnitude of attenuation between this 1st terminal and this 2nd terminal may be changed. This 1st terminal It connects with this 3rd terminal and this 1st terminal is intercepted from this 2nd terminal. This 2nd terminal So that it connects with a ground, and the magnitude of attenuation between this 1st terminal and this 3rd terminal may be changed, the impedance Z1 seen from this 1st terminal maintaining equal relation substantially to the impedance Z3 seen from this 3rd terminal This switch attenuator is electrically controllable and the above-mentioned purpose is attained by that.

[0013] With a certain operation gestalt, the 1st transistor is prepared between said 1st terminal and grounds. The 2nd transistor is prepared between said 2nd terminal and grounds. The 3rd transistor is prepared between said 3rd terminal and grounds. The 4th transistor is prepared between this 1st terminal and this 2nd terminal, the 5th transistor is prepared between this 1st terminal and this 3rd terminal, and it sets in said 1st condition. This 3rd transistor is an ON state, this 5th transistor is an OFF state, in said 2nd condition, this 3rd transistor is an ON state and this 5th transistor is an OFF state.

[0014] With a certain operation gestalt, it is contained substantially [said impedance Z1] in the range of $0.5 \times ZA - 2.0 \times ZA$, is contained substantially [said impedance Z2] in the range of $0.5 \times ZT - 2.0 \times ZT$, and is contained substantially [said impedance Z3] in the range of $0.5 \times ZR - 2.0 \times ZR$, and ZA, ZT, and ZR express the impedance of said antenna, said transmitter, and said receiver here, respectively.

[0015] With a certain operation gestalt, each of said 1st transistor, said 2nd transistor, said 3rd transistor, said 4th transistor, and said 5th transistor the dual gate field-effect transistor which has a drain, the source, and the two gates -- it is -- this -- one gate of the two gates it connects with this drain -- having -- **** -- this -- the gate of another side of the two gates is connected to this source -- having -- **** -- this -- the two gates receive the electrical potential difference for electric control through resistance, respectively.

[0016] The 1st terminal by which the switch attenuator by this invention is connected to the 1st antenna, It has the 2nd terminal connected to a transmitter, the 3rd terminal connected to a receiver, and the 4th terminal connected to the 2nd antenna. Are the switch attenuator which changes the 1st condition, the 2nd condition, the 3rd condition, and the 4th condition, and it sets in this 1st condition. It connects with this 2nd terminal, and this 1st terminal is intercepted from this 3rd terminal. This 3rd terminal Connect with a ground and this 4th terminal is intercepted from

this 1st terminal, this 2nd terminal, this 3rd terminal, and this ground. The impedance Z1 seen from this 1st terminal maintaining equal relation substantially to the impedance Z2 seen from this 2nd terminal, so that the magnitude of attenuation between this 1st terminal and this 2nd terminal may be changed This switch attenuator is electrically controllable and it sets in this 2nd condition. It connects with this 3rd terminal, and this 1st terminal is intercepted from this 2nd terminal. This 2nd terminal Connect with a ground and this 4th terminal is intercepted from this 1st terminal, this 2nd terminal, this 3rd terminal, and this ground. The impedance Z1 seen from this 1st terminal maintaining equal relation substantially to the impedance Z3 seen from this 3rd terminal, so that the magnitude of attenuation between this 1st terminal and this 3rd terminal may be changed This switch attenuator is electrically controllable and it sets in this 3rd condition. It connects with this 2nd terminal, and this 4th terminal is intercepted from this 3rd terminal. This 3rd terminal Connect with a ground and this 1st terminal is intercepted from this 2nd terminal, this 3rd terminal, this 4th terminal, and this ground. The impedance Z4 seen from this 4th terminal maintaining equal relation substantially to the impedance Z2 seen from this 2nd terminal, so that the magnitude of attenuation between this 4th terminal and this 2nd terminal may be changed This switch attenuator is electrically controllable and it sets in this 4th condition. It connects with this 3rd terminal, and this 4th terminal is intercepted from this 2nd terminal. This 2nd terminal Connect with a ground and this 1st terminal is intercepted from this 2nd terminal, this 3rd terminal, this 4th terminal, and this ground. The impedance Z4 seen from this 4th terminal maintaining equal relation substantially to the impedance Z3 seen from this 3rd terminal, so that the magnitude of attenuation between this 4th terminal and this 3rd terminal may be changed This switch attenuator is electrically controllable and the above-mentioned purpose is attained by that.

[0017] With a certain operation gestalt, the 1st transistor is prepared between said 1st terminal and grounds. The 2nd transistor is prepared between said 2nd terminal and grounds. The 3rd transistor is prepared between said 3rd terminal and grounds. The 4th transistor is prepared between this 1st terminal and this 2nd terminal. The 5th transistor It is prepared between this 1st terminal and this 3rd terminal, and the 6th transistor is prepared between said 4th terminal and grounds. The 7th transistor is prepared between this 2nd terminal and this 4th terminal, the 8th transistor is prepared between this 3rd terminal and this 4th terminal, and it sets in said 1st condition. This 3rd transistor is an ON state. This 5th transistor, this 6th transistor, this 7th transistor, and this 8th transistor It is an OFF state and sets in said 2nd condition. This 2nd transistor It is an ON state. This 4th transistor, this 6th transistor, this 7th transistor, and this 8th transistor It is an OFF state and sets in said 3rd condition. This 3rd transistor It is an ON state. This 1st transistor, this 4th transistor, this 5th transistor, and this 8th transistor It is an OFF state, and in said 4th condition, this 2nd transistor is an ON state and this 1st transistor, this 4th transistor, this 5th transistor, and this 7th transistor are OFF states.

[0018] With a certain operation gestalt, it is contained substantially [said impedances Z1 and Z4] in the range of 0.5xZA-2.0xZA, is contained substantially [said impedance Z2] in the range of 0.5xZT-2.0xZT, and is contained substantially [said impedance Z3] in the range of 0.5xZR-2.0xZR, and ZA, ZT, and ZR express the impedance of said antenna, said transmitter, and said receiver here, respectively.

[0019] With a certain operation gestalt, on the semi-conductor substrate, it integrates and is formed.

[0020] With a certain operation gestalt, it has power amplifier further, and this power amplifier is integrated and formed on said semi-conductor substrate.

[0021] With a certain operation gestalt, it has the low noise amplifier further, and this low noise amplifier is integrated and formed on said semi-conductor substrate.

[0022]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained, referring to a drawing. The same reference mark expresses the same component.

[0023] The "switch attenuator" in this specification says the equipment it has equipment and the function of RF switch for antennas, and RF attenuator so that it may mention later. Moreover, a "node" does not necessarily need the terminal for connection with the equipment exterior.

[0024] (Gestalt 1 of operation) Drawing 3 is the block diagram of the RF section 30 of the portable telephone with which the 1st operation gestalt of the switch attenuator of this invention is used. The switch attenuator 40 of this invention combines electrically an antenna 130, and power amplifier 116 or a low noise amplifier 152 according to the condition of transmission and reception. The switch attenuator 40 combines a node T1 with a node T2 electrically at the time of transmission, and, more specifically, combines node T3 with a ground electrically. Moreover, the switch attenuator 40 combines a node T1 with node T3 electrically at the time of reception, and combines a node T2 with a ground electrically. The ground in this specification is connected to the case shielded in RF while the negative

electrode of a power source is connected and it offers common potential about the both sides of a direct-current (referred to as "DC" below) signal, and a RF signal. The flow of the signal at the time of the transmission and reception in the RF section 30 is the same as drawing 1 explained.

[0025] Since the switch attenuator 40 by this invention has a switch and the function of an attenuator so that it may mention later, it has the big effectiveness that the AGC amplifier 114 and attenuator 150 of drawing 1 can be lost. Moreover, if it manufactures as a semiconductor device which had the switch attenuator 40 unified, drastic reduction of size and cost is more desirable than a possible next door. In addition, all the transmission lines that connect each block of drawing 3 have the characteristic impedance of 50 ohms. Moreover, although the RF section 30 is used as some portable telephones, it is not limited to this here. The RF section 30 can be widely used for the equipment which transmits and receives a RF signal, and it can use the switch attenuator 40 widely as equipment to attenuate while changing a RF signal.

[0026] In drawing 3, the control voltage generator valve flow coefficient 1 is generated based on the data in which the control voltage for setting up the condition of FET contained in the switch attenuator 40 as shown in Table 1 - 4 explained later was stored by the read only memory ROM 1, and is supplied to each FET. A read only memory ROM 1 stores the data for generating the control voltage of FET corresponding to the condition of Table 1 - 4.

[0027] Drawing 4 is the circuit diagram of the 1st operation gestalt of the switch attenuator by this invention. The switch attenuator 40 is equipped with nodes T1 and T2 and T3, and is connected to an antenna 130, power amplifier 116, and a low noise amplifier 152, respectively. The control voltage generator valve flow coefficient 1 generates the electrical potential difference which controls FET based on the data stored in the read only memory ROM 1, and outputs it to nodes CT1-CT5.

[0028] FET Q1 connects a node T1 to a ground with a certain impedance. The control voltage received in the node CT 1 minds resistance R12, and is FET. It is added to the gate of Q1 and is FET. This predetermined impedance of Q1 is changed. It responds to the control voltage of a node CT 1, and, specifically, is FET. Q1 can take the impedance of the large range from an ON state to an OFF state. FET In an ON state, the impedance of Q1 is low to extent it can consider that is zero, and high to extent it can consider that is infinite in an OFF state. FET Since it is the depletion type of N type, Q1 is FET. It is FET conversely that what is necessary is just to give the electrical potential difference Vgs between the gate sources more than 0 [V] in order to make Q1 into an ON state. What is necessary is just to give the electrical potential difference Vgs between the gate sources below a threshold VTH [V] ($VTH < 0$), in order to make Q1 into an OFF state. FET When filling the relation which the electrical potential difference Vgs between the gate sources of Q1 becomes $VTH < Vgs < 0$, it sets on these specifications, and it is FET. Q1 is made to call that it is the "intermediate state" of an ON state and an OFF state. FET Q1 is the Schottky barrier gate mold FET (referred to as "MESFET" below) with the gestalt of this operation. As mentioned above, FET It sets on these specifications and the explanation about Q1 is FET. It is applied also about Q2-Q4.

[0029] FET It is FET like Q1. Q2 and Q3 connect a node T2 and T3 to a ground with a certain impedance, respectively. The control voltage received in nodes CT2 and CT3 minds resistance R22, and is FET, respectively. Resistance R32 is minded [of Q2] again, and it is FET. It is added to the gate of Q3 and is FET, respectively. The impedance of Q2 and Q3 is changed. Resistance R12, R22, and R32 is resistance for gate bias.

[0030] FET Between the source of Q1, Q2, and Q3, and a ground, resistance R11, R21, and R31 is formed, respectively. These resistance R11, R21, and R31 is FET, respectively. Impedance matching is taken by adjusting the nodes T1 and T2 in case Q1, Q2, and Q3 are ON states, and the impedance between T3 and a ground.

[0031] FET It is FET like Q1. Q4 and Q5 connect a node T2 and T3 to a node T1 with a certain impedance, respectively. The control voltage received in nodes CT4 and CT5 minds resistance R42, respectively, and is FET. Resistance R52 is minded [of Q4] again, and it is FET. It is added to the gate of Q5 and the impedance of FETQ4 and Q5 is changed, respectively.

[0032] Next, actuation of the switch attenuator 40 is explained. The switch attenuator 40 has the following modes of operation 1-4. Namely, transmission without mode 1:attenuation, transmission with mode 2:attenuation, the reception without mode 3:attenuation, and the mode 4: It is reception with attenuation. Attenuation between a node T1, and a node T2 or node T3 of "attenuation" is said here. For example, in the mode 1, attenuation between a node T1 and a node T2 does not exist. The mode 1 is used when the migration terminal containing the RF section 30 is distant from the base station (i.e., when supplying an antenna 130, without attenuating the RF signal outputted from power amplifier 116). The mode 2 is used when the migration terminal which contains the RF section 30 conversely is close to a base station (i.e., since the RF signal outputted from power amplifier 116 is attenuated when supplying an antenna 130). It is applied also when it is reception that it is the same as that of the case of transmission. The mode

3 is used when the migration terminal containing the RF section 30 is distant from the base station (i.e., when supplying a low noise amplifier 152, without attenuating the RF signal inputted from the antenna 130). The mode 4 is used when the migration terminal which contains the RF section 30 conversely is close to a base station (i.e., since the RF signal inputted from the antenna 130 is attenuated when supplying a low noise amplifier 152).

[0033] The switch attenuator 40 of this invention can change the magnitude of attenuation of the switch attenuator 40 continuously by changing the control voltage of a switching element (here FET) in the mode 2 and the mode 4 so that it may mention later. Consequently, the switch attenuator of this invention does big effectiveness so in the mobile communication which can take a range with large output power at the time of transmission and input power at the time of reception.

[0034] (Mode 1) FET of the switch attenuator 40 in the mode 1 The condition of Q1-Q5 is shown in Table 1.

[0035]

[Table 1]

FET	Q1	Q2	Q3	Q4	Q5
状態	オフ	オフ	オン	オン	オフ

[0036] It is FET in order to realize the mode 1 of the switch attenuator 40. What is necessary is just to impress the control voltage corresponding to each condition of setting Q1-Q5 as the condition which shows in Table 1 to nodes CT1-CT5. It is FET as mentioned above. It is FET that what is necessary is just to apply the electrical potential difference for example, more than 0 [V] to each gate in order to make Q1-Q5 into an ON state. What is necessary is just to apply the electrical potential difference for example, below VTH [V] to each gate, in order to make Q1-Q5 into an OFF state.

[0037] Drawing 5 is the representative circuit schematic of the switch attenuator 40 in the mode 1. In drawing 5 , the closed switch expresses FET of an ON state and the open switch expresses FET of an OFF state. As the mode 1 is shown in drawing 5 , an impedance is mostly connected to a node T2 by zero, as for node T3, an impedance is mostly connected to a ground by zero, and node T3 is intercepted for the node T1 from the node T1 and the node T2. Therefore, the RF signal outputted from power amplifier 116 in the mode 1 is FET, without receiving and decreasing in a node T2. An antenna 130 is supplied through Q4 and a node T1. Moreover, node T3 which is an input terminal to a low noise amplifier 152 is FET. It prevents Q's3 connecting with a ground and an unnecessary RF signal being inputted by that cause into a low noise amplifier 152.

[0038] The insertion loss of the switch attenuator 40 in the mode 1 is FET. It is only about 0.5dB resulting from the impedance (that is, impedance equivalent to on resistance) of the ON state of Q4.

[0039] (Mode 2) FET of the switch attenuator 40 in the mode 2 The condition of Q1-Q5 is shown in Table 2.

[0040]

[Table 2]

FET	Q1	Q2	Q3	Q4	Q5
状態	中間	中間	オン	中間	オフ

[0041] It is FET in order to realize the mode 2 of the switch attenuator 40. What is necessary is just to impress the control voltage corresponding to each condition of setting Q1-Q5 as the condition which shows in Table 2 to nodes CT1-CT5. In the mode 2 and the mode 4, FET is used by the intermediate state. FET What is necessary is just to apply to each gate the electrical potential difference which becomes $0 < V_{gs} < V_{TH}$ as an electrical potential difference V_{gs} between the gate sources, in order to make Q1-Q5 into an intermediate state.

[0042] Drawing 6 is the representative circuit schematic of the switch attenuator 40 in the mode 2. In drawing 6 , the closed switch expresses FET of an ON state, the open switch expresses FET of an OFF state, and resistance expresses FET of an intermediate state. Hereafter, the impedance of FETQ1-Q5 of an intermediate state is made to express like ZQ1-ZQ5, respectively. As the mode 2 is shown in drawing 6 , it connects with a node T2 with an impedance ZQ4, and a node T1 is connected to a ground with an impedance ZQ1. A node T2 is connected to a ground with an impedance ZQ2. As for node T3, an impedance is mostly connected to a ground by zero, and node T3 is intercepted from the node T1 and the node T2. Therefore, it is received in a node T2, it is accompanied by the desired magnitude of attenuation, and the RF signal outputted from power amplifier 116 in the mode 2 is FET. An antenna 130 is supplied through Q1, Q2, Q4, and a node T1. Moreover, node T3 which is an input terminal to a low noise amplifier 152 is FET. It prevents Q's3 connecting with a ground and an unnecessary RF signal being inputted by

that cause into a low noise amplifier 152.

[0043] The magnitude of attenuation of the switch attenuator 40 in the mode 2 is FET. It changes changing the control voltage applied to the gate of Q1, Q2, and Q4, i.e., by changing impedances ZQ1, ZQ2, and ZQ4. The value of the control voltage applied to the gate of FETQ1, Q2, and Q4 is beforehand stored in the read only memory ROM 1, for example, and is read according to the required magnitude of attenuation. For example, if the control voltage generator valve flow coefficient 1 which is a programmable voltage generator generates control voltage based on the data showing the control voltage read from ROM1 and outputs to the gate of each FET, the mode 2 and the mode 4 only for a desired amount to attenuate a RF signal are realizable. Moreover, ROM1 is FET. The data showing the control voltage (that is, the electrical potential difference more than each 0 [V] and the electrical potential difference below VTH [V]) applied to the gate of Q3 and Q5 may be stored collectively. Furthermore, it sets in the modes 1, 3, and 4, and ROM1 is FET. The data showing the control voltage applied to Q1-Q5 may be stored collectively.

[0044] (Mode 3) FET of the switch attenuator 40 in the mode 3 The condition of Q1-Q5 is shown in Table 3.

[0045]

[Table 3]

FET	Q1	Q2	Q3	Q4	Q5
状態	オフ	オン	オフ	オフ	オン

[0046] It is FET in order to realize the mode 3 of the switch attenuator 40. What is necessary is just to impress the control voltage corresponding to each condition of setting Q1-Q5 as the condition which shows in Table 3 to nodes CT1-CT5.

[0047] Drawing 7 is the representative circuit schematic of the switch attenuator 40 in the mode 3. As the mode 3 is shown in drawing 7 R> 7, an impedance is mostly connected to node T3 by zero, mostly, an impedance is connected to a ground by zero and the node T2 is intercepted [the node T2] for the node T1 from a node T1 and node T3. Therefore, the RF signal inputted from the antenna 130 in the mode 3 is FET, without receiving and decreasing in a node T1. A low noise amplifier 152 is supplied through Q5 and node T3. Moreover, the node T2 which is an output terminal from power amplifier 116 is FET. It prevents Q's2 connecting with a ground and an unnecessary RF signal being outputted by that cause to a low noise amplifier 152.

[0048] The insertion loss of the switch attenuator 40 in the mode 3 is FET. It is only about 0.5dB resulting from the impedance of the ON state of Q5.

[0049] (Mode 4) FET of the switch attenuator 40 in the mode 4 The condition of Q1-Q5 is shown in Table 4.

[0050]

[Table 4]

FET	Q1	Q2	Q3	Q4	Q5
状態	中間	オン	中間	オフ	中間

[0051] It is FET in order to realize the mode 4 of the switch attenuator 40. What is necessary is just to impress the control voltage corresponding to each condition of setting Q1-Q5 as the condition which shows in Table 4 to nodes CT1-CT5.

[0052] Drawing 8 is the representative circuit schematic of the switch attenuator 40 in the mode 4. As the mode 4 is shown in drawing 8 R> 8, it connects with node T3 with an impedance ZQ5, and a node T1 is connected to a ground with an impedance ZQ1. Node T3 is connected to a ground with an impedance ZQ3. Mostly, an impedance is connected to a ground by zero, and the node T2 is intercepted for the node T2 from a node T1 and node T3. Therefore, it is received in a node T1, it is accompanied by the desired magnitude of attenuation, and the RF signal inputted from the antenna 130 in the mode 4 is FET. A low noise amplifier 152 is supplied through Q1, Q3, Q5, and node T3. Moreover, the node T2 which is an output terminal from power amplifier 116 is FET. It prevents Q's2 connecting with a ground and an unnecessary RF signal being inputted by that cause into a low noise amplifier 152.

[0053] The magnitude of attenuation of the switch attenuator 40 in the mode 4 is FET. It changes changing the control voltage applied to the gate of Q1, Q3, and Q5, i.e., by changing impedances ZQ1, ZQ3, and ZQ5. The value of the control voltage applied to the gate of FETQ1, Q3, and Q5 is beforehand stored in the read only memory ROM 1, as explained in the mode 2, and it is read according to the required magnitude of attenuation.

[0054] The magnitude of attenuation can be changed filling the relation it is substantially unrelated $ZT1=ZT2=Z0$ in the mode 2 according to the gestalt of the 1st operation. An impedance ZT1 expresses the impedance of the switch

attenuator 40 seen from the node T1, an impedance ZT2 expresses the impedance of the switch attenuator 40 seen from the node T2, and an impedance Z0 expresses the characteristic impedance (for example, 50ohms) of the circuit connected outside here. The magnitude of attenuation can be changed filling similarly the relation it is substantially unrelated $ZT1=ZT3=Z0$ in the mode 4 according to the gestalt of the 1st operation. An impedance ZT3 expresses the impedance of the switch attenuator 40 seen from node T3 here.

[0055] Moreover, even if above-mentioned $ZT1=ZT2=Z0$ and the relation it is unrelated $ZT1=ZT3=Z0$ are not filled, it is desirable that relation called $0.5 \times ZA \leq ZT1 \leq 2.0 \times ZA$, $0.5 \times ZT \leq ZT2 \leq 2.0 \times ZT$, and $0.5 \times ZR \leq ZT3 \leq 2.0 \times ZR$ is filled. An impedance ZA expresses the characteristic impedance of the circuit (here antenna 130) connected to a node T1, an impedance ZT expresses the characteristic impedance of the circuit (here power amplifier 116) connected to a node T2, and an impedance ZR expresses the characteristic impedance of the circuit (here low noise amplifier 152) connected to node T3 here.

[0056] Drawing 9 is the top view of the switch attenuator 40 of this invention integrated and formed on the semiconductor substrate. As shown in drawing 9, the switch attenuator 40 is integrated and formed on the gallium-arsenide (referred to as "GaAs" below) substrate 901. "GND" of drawing 9 expresses a ground and other reference marks correspond with them in drawing 4. FET Q1-Q5 are MESFET(s), and they are formed by ion-implantation on the GaAs substrate 901. FET Gate length is 0.5 micrometers and the gate width of the size of Q1-Q5 is 800 micrometers. The closure of the semiconductor chip which realized the switch attenuator 40 shown in drawing 9 is carried out to the resin mold package of ten pins, and it is made available.

[0057] (Gestalt 2 of operation) Drawing 10 is the circuit diagram of the 2nd operation gestalt of the switch attenuator by this invention. FET of drawing 10 Q1D, Q2D, Q3D, Q4D, and Q5D are dual gate FET. FET The gate bias resistors R13 and R14, R23 and R24, R33 and R34, R43 and R44, and R53 and R54 are connected to the 1st gate and the 2nd gate of Q1 D-Q5D, respectively. Moreover, FET Between the 2nd gate of Q1D – Q5D, and a drain, capacitors C13, C23, C33, C43, and C53 are connected, respectively, and it is FET. Between the 1st gate of Q1 D-Q5D, and the source, capacitors C14, C24, C34, C44, and C54 are connected, respectively.

[0058] As for the 2nd operation gestalt, it differs from the 1st operation gestalt that the capacitor is connected between that dual gate FET is used instead of, and a drain and the 2nd gate and between the source and the 1st gate. [a single gate FET] According to the configuration of the 2nd operation gestalt, the nonlinearity which FET has can be reduced and the outstanding distorted property can be realized.

[0059] (Gestalt 3 of operation) Drawing 11 is the block diagram of the RF section 1100 of the portable telephone with which the 3rd operation gestalt of the switch attenuator of this invention is used. The switch attenuator 1200 of this invention combines electrically antennas 130 or 131, and power amplifier 116 or a low noise amplifier 152 according to the condition of transmission and reception.

[0060] More specifically, the switch attenuator 1200 intercepts the node which one is electrically combined with a node T2 of a node T1 and the T four at the time of transmission, combines node T3 with a ground electrically, and is not combined with a node T2 among a node T1 and T four from other nodes and grounds.

[0061] Moreover, the switch attenuator 1200 intercepts the node which one is electrically combined with node T3 of a node T1 and the T four at the time of reception, combines a node T2 with a ground electrically, and is not combined with node T3 among a node T1 and T four from other nodes and grounds. Unlike having used the antenna with the 1st single operation gestalt, the 3rd operation gestalt can use two antennas 130 and 131. Therefore, in addition to the effectiveness of the 1st operation gestalt, the 3rd operation gestalt has the effectiveness that two antennas 130 and 131 can be alternatively used according to the situation of transmission and reception. The configuration of this 3rd operation gestalt enables for example, space diversity transmission and reception. In addition, all the transmission lines that connect each block of drawing 11 have the characteristic impedance of 50 ohms.

[0062] The control voltage generator valve flow coefficient 2 in drawing 11 and drawing 12 and a read only memory ROM 2 function as the control voltage generator valve flow coefficient 1 and a read only memory ROM 1 similarly except for the nodes which supply the electrical potential difference which controls FET being CT1-CT8.

[0063] Drawing 12 is the circuit diagram of the 3rd operation gestalt of the switch attenuator by this invention. In order to join together electrically of a node T2 and T3 to one, the switch attenuator 1200 adds node T four to the component of the switch attenuator 40, and is FET. It has further Q6-Q8, the resistance R62, R72, and R82 for gate bias, nodes CT6-CT8, and the resistance R61 for impedance matching.

[0064] Next, actuation of the switch attenuator 1200 is explained. The switch attenuator 1200 has the following modes of operation 1-8. Namely, the transmission without attenuation using the mode 1:antenna 130, the mode 2 :

The transmission with attenuation using an antenna 130, Mode 3 : The reception without attenuation using an antenna 130, the reception with attenuation using the mode 4:antenna 130, mode 5: -- they are the transmission without attenuation using an antenna 131, the transmission with attenuation using the mode 6:antenna 131, the reception without attenuation using the mode 7:antenna 131, and reception with attenuation using the mode 8:antenna 131. The modes 1–4 of the 3rd operation gestalt are equivalent to the mode 1 of the 1st operation gestalt – the mode 4, respectively. Node T four of the modes 5–8 of the 3rd operation gestalt is the same as that of the modes 1–4 except for being electrically combined with a node T2 or T3 instead of a node T1.

[0065] What is necessary is just to impress the control voltage corresponding to each condition of setting FETQ1–Q8 as the condition which shows in following Table 5 – 12, respectively to nodes CT1–CT8, in order to realize the modes 1–8 of the switch attenuator 1200. The representative circuit schematic in the mode 1 of the switch attenuator 1200 – the mode 8 is shown in drawing 13 – drawing 20 , respectively.

[0066]

[Table 5]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オフ	オン	オン	オフ	オフ	オフ	オフ

[0067]

[Table 6]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	中間	中間	オン	中間	オフ	オフ	オフ	オフ

[0068]

[Table 7]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オン	オフ	オフ	オン	オフ	オフ	オフ

[0069]

[Table 8]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	中間	オン	中間	オフ	中間	オフ	オフ	オフ

[0070]

[Table 9]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オフ	オン	オフ	オフ	オフ	オン	オフ

[0071]

[Table 10]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	中間	オン	オフ	オフ	中間	中間	オフ

[0072]

[Table 11]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オン	オフ	オフ	オフ	オフ	オフ	オン

[0073]

[Table 12]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オン	中間	オフ	オフ	中間	オフ	中間

[0074] With the gestalt of the 3rd operation, the magnitude of attenuation can be changed like the gestalt of the 1st operation, filling substantially $ZT1=ZT2=Z0$ and the relation it is unrelated $ZT1=ZT3=Z0$ in the modes 2 and 4, respectively. Moreover, with the gestalt of the 3rd operation, the magnitude of attenuation can be changed in the modes 6 and 8, filling substantially $ZT4=ZT2=Z0$ and the relation it is unrelated $ZT4=ZT3=Z0$, respectively. An impedance $ZT4$ expresses the impedance of the switch attenuator 1200 seen from node T four here.

[0075] Moreover, even if the above-mentioned $ZT1=ZT2=Z0$, $ZT1=ZT3=Z0$, $ZT4=ZT2=Z0$, and the relation it is unrelated $ZT4=ZT3=Z0$ are not filled, it is desirable that relation called $0.5xZA \leq ZT1 \leq 2.0xZA$, $0.5xZT \leq ZT2 \leq 2.0xZT$, $0.5xZR \leq ZT3 \leq 2.0xZR$, and $0.5xZB \leq ZT4 \leq 2.0xZB$ is filled. An impedance ZB expresses the characteristic impedance of the circuit (here antenna 131) connected to node T four here.

[0076] With the gestalt of the 1st explained above – the 3rd operation, by setting FET as the middle condition of ON and OFF, also when the property of the circuit connected to a switch attenuator changes, it can respond flexibly. Such property change of the circuit connected may take place, when changing the power outputted from the power amplifier for transmission.

[0077] Although a desired characteristic impedance is obtained with the gestalt of the above-mentioned implementation in the frequency band used, for example by the communication link between a portable telephone and a base station, it is not limited to this frequency band, but can apply to RF band widely.

[0078] Based on the indication of the gestalt of the 2nd operation, the further effectiveness that the outstanding distorted property is realizable can also be acquired by transposing FET of the gestalt of the 3rd operation to dual gate FET.

[0079] FET used for the switch attenuator of this invention is not limited to a depletion type, but an enhancement type may be used for it. Moreover, FET should just be the device which is not limited to this although it is MESFET, but can control an impedance by the above-mentioned operation gestalt electrically with the control terminal. As long as conditions, such as an operating frequency and parasitic capacitance of a device proper, allow, a PIN diode, the PN-junction mold FET, a MOSFET, etc. may be used, for example.

[0080] Moreover, if the switch attenuator by this invention is integrated and formed on a semi-conductor substrate with power amplifier or a low noise amplifier, reduction of size and cost can be aimed at and it is more desirable.

[0081] The control voltage generators valve flow coefficient1 and valve flow coefficient2 and read only memories ROM1 and ROM2 will not be restricted to the configuration explained with the gestalt of the above-mentioned implementation, if the control voltage for setting the condition of FET of the switch attenuator by this invention as the condition of either an ON state, an intermediate state and an OFF state can be generated. For example, a programmable voltage generator without the memory which stores data in digital one may be used. Moreover, random access memory may be used instead of read only memories ROM1 and ROM2.

[0082] As shown in Table 2, Table 4, Table 6, and Table 8, 10, and 12, with the gestalt of above-mentioned operation, three FET is set as an intermediate state at the time of the transmission with attenuation, or reception. However, the number of FET of an intermediate state is not restricted to three pieces, but when at least one FET is an intermediate state, the desired magnitude of attenuation should just be obtained.

[0083]

[Effect of the Invention] As mentioned above, according to this invention, in a RF device, controlling the magnitude of attenuation freely to the change sexagenary-cycle coincidence of the change of transmission and reception or two or more antennas can be realized by one semiconductor device, and the remarkable effectiveness that the formation of small lightweight and low-cost-izing of a device can be attained is acquired.

[Translation done.]

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the switch attenuator containing the high frequency switch and high frequency attenuator which are used for a high frequency transceiver circuit. Moreover, this invention relates to the semiconductor device which realizes this switch attenuator, and the RF device using this semiconductor device.

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PRIOR ART

[Description of the Prior Art] Drawing 1 is the block diagram showing the high frequency (referred to as "RF" below) section 10 of the transceiver circuit by the Prior art. The RF section 10 of a transceiver circuit is equipped with the RF switch 120, and, thereby, performs transmission and reception alternatively. At the time of transmission, the signal inputted in the modulating-signal input terminal (MOD in) 110 is radiated from an antenna 130 in space through a frequency converter (it considers as a "mixer" below) 112, a variable gain amplifier (it considers as "AGC amplifier" below) 114, power amplifier (PA) 116, the RF switch (RF SW) 120, and the frequency filter 122.

[0003] Conversely, at the time of reception, the signal received in the antenna 130 is outputted through the frequency filter 122, the RF switch 120, an attenuator 150, a low noise amplifier (LNA) 152, and a mixer 154 from the intermediate frequency (referred to as "IF" below) signal output terminal (IF out) 156.

[0004] transmission and reception -- in any case, a local oscillation signal with a desired frequency is generated, and a phase locked loop (referred to as "PLL" below) 170 and an oscillator 172 output it to a signal distribution box (DIV) 174. By mixing a modulating signal and a local oscillation signal, a mixer 112 generates a RF signal and outputs it to the AGC amplifier 114. By mixing a RF signal and a local oscillation signal, a mixer 154 generates an IF signal and outputs it to the IF signal output terminal 156.

[0005] Actuation of the RF section 10 of drawing 1 is explained below. The RF sections 10 are some mobile transmitters represented by the terminal of a cellular phone. In almost all cases, in a mobile transmitter, the antenna 130 (here, it thinks also including the frequency filter 122) which requires the comparatively big volume for simplification of configuration is used for the both sides of a sending circuit and a receiving circuit. In order to share the antenna section by transmission and reception, at the time of transmission, it is electrically combined with power amplifier 116, and an antenna 130 is electrically separated from a low noise amplifier 152. Conversely, at the time of reception, it dissociates from power amplifier 116 electrically, and an antenna 130 is electrically combined with a low noise amplifier 152. In order to perform the change for such transmission and reception, the semiconductor-device-ized RF switch 120 is usually adopted. The RF switch 120 by the conventional technique uses the transistor as a switching element, and it is controlling it electrically so that a transistor takes the condition of either an ON state and an OFF state.

[0006] Moreover, the terminal (for example, the hand set of a cellular phone itself) in mobile communications transmits a RF signal to a nearby base station, and communicates by receiving a RF signal from a base station. In order to maintain the power received in a base station to about 1 law, according to the distance of a terminal and a base station, it is necessary to control delicately the power transmitted from a terminal. In order to maintain almost uniformly the power outputted in the IF signal output terminal 156 of a terminal on the contrary, it is necessary to control RF power inputted into a low noise amplifier 152. In order to fill these demands, generally the RF section 10 of a terminal is equipped with the AGC amplifier 114 for transmission, and the attenuator 150 for reception.

[0007] Drawing 2 is the circuit diagram of the switch 20 by the Prior art. The switch 20 is equipped with field-effect transistors (referred to as "FET" below) 200-203, the resistors 210 and 211 for impedance adjustment, the gate bias resistors 220-223, the antenna terminal 230, the transmitted power-input terminal 231, the received-power output terminal 232, the 1st control terminal 245, and the 2nd control terminal 246 in drawing 2.

[0008] Actuation of the switch of drawing 2 is explained. At the time of transmission, by impressing a negative larger electrical potential difference than the absolute value of the threshold of FET 201 and 202 to the 2nd control terminal 246, FET 201 and 202 is made into an OFF state, and zero or a forward electrical potential difference is impressed to the 1st control terminal 245, and FET 200 and 203 is made into an ON state. Thereby, transmitted power passes along a terminal 231, FET200, and the antenna terminal 230, and is outputted to an antenna 250.

[0009] Conversely, at the time of reception, by impressing a negative larger electrical potential difference than the

absolute value of the threshold of FET 200 and 203 to the 1st control terminal 245, FET 200 and 203 is made into an OFF state, and zero or a forward electrical potential difference is impressed to the 2nd control terminal 246, and FET 201 and 202 is made into an ON state. Thereby, received power passes along an antenna 250, a terminal 230, and FET201, and is outputted to a terminal 232.

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EFFECT OF THE INVENTION

[Effect of the Invention] As mentioned above, according to this invention, in a RF device, controlling the magnitude of attenuation freely to the change sexagenary-cycle coincidence of the change of transmission and reception or two or more antennas can be realized by one semiconductor device, and the remarkable effectiveness that the formation of small lightweight and low-cost-izing of a device can be attained is acquired.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] In the migration terminal equipment of a cellular phone, in order to raise portability, while lightweight[small and]-izing a device, low-cost-izing is important. In order to realize this, the miniaturization and low-cost-izing of a circuit in current and the RF section are called for strongly. However, also in which the above-mentioned conventional technique, the transceiver circuit needed to have a switch, AGC amplifier, and an attenuator separately. Consequently, it had the technical problem that the transceiver circuit by the Prior art had the size of a device, and unescapable increase of cost.

[0011] The place which it is made in order that this invention may solve the above-mentioned technical problem, and is made into the purpose is to offer the equipment which functions as small [which is used for a high frequency transceiver circuit], a light and low cost switch, and an attenuator.

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MEANS

[Means for Solving the Problem] The 1st terminal by which the switch attenuator by this invention is connected to an antenna, Have the 2nd terminal connected to a transmitter, and the 3rd terminal connected to a receiver, and are the switch attenuator which changes the 1st condition and the 2nd condition, and it sets in this 1st condition. This 1st terminal is connected to this 2nd terminal. This 1st terminal The impedance Z1 which it was intercepted from this 3rd terminal, and this 3rd terminal was connected to the ground, and was seen from this 1st terminal maintaining equal relation substantially to the impedance Z2 seen from this 2nd terminal This switch attenuator is electrically controllable and it sets in this 2nd condition so that the magnitude of attenuation between this 1st terminal and this 2nd terminal may be changed. This 1st terminal It connects with this 3rd terminal and this 1st terminal is intercepted from this 2nd terminal. This 2nd terminal So that it connects with a ground, and the magnitude of attenuation between this 1st terminal and this 3rd terminal may be changed, the impedance Z1 seen from this 1st terminal maintaining equal relation substantially to the impedance Z3 seen from this 3rd terminal This switch attenuator is electrically controllable and the above-mentioned purpose is attained by that.

[0013] With a certain operation gestalt, the 1st transistor is prepared between said 1st terminal and grounds. The 2nd transistor is prepared between said 2nd terminal and grounds. The 3rd transistor is prepared between said 3rd terminal and grounds. The 4th transistor is prepared between this 1st terminal and this 2nd terminal, the 5th transistor is prepared between this 1st terminal and this 3rd terminal, and it sets in said 1st condition. This 3rd transistor is an ON state, this 5th transistor is an OFF state, in said 2nd condition, this 3rd transistor is an ON state and this 5th transistor is an OFF state.

[0014] With a certain operation gestalt, it is contained substantially [said impedance Z1] in the range of $0.5 \times ZA - 2.0 \times ZA$, is contained substantially [said impedance Z2] in the range of $0.5 \times ZT - 2.0 \times ZT$, and is contained substantially [said impedance Z3] in the range of $0.5 \times ZR - 2.0 \times ZR$, and ZA, ZT, and ZR express the impedance of said antenna, said transmitter, and said receiver here, respectively.

[0015] With a certain operation gestalt, each of said 1st transistor, said 2nd transistor, said 3rd transistor, said 4th transistor, and said 5th transistor the dual gate field-effect transistor which has a drain, the source, and the two gates -- it is -- this -- one gate of the two gates it connects with this drain -- having -- **** -- this -- the gate of another side of the two gates is connected to this source -- having -- **** -- this -- the two gates receive the electrical potential difference for electric control through resistance, respectively.

[0016] The 1st terminal by which the switch attenuator by this invention is connected to the 1st antenna, It has the 2nd terminal connected to a transmitter, the 3rd terminal connected to a receiver, and the 4th terminal connected to the 2nd antenna. Are the switch attenuator which changes the 1st condition, the 2nd condition, the 3rd condition, and the 4th condition, and it sets in this 1st condition. It connects with this 2nd terminal, and this 1st terminal is intercepted from this 3rd terminal. This 3rd terminal Connect with a ground and this 4th terminal is intercepted from this 1st terminal, this 2nd terminal, this 3rd terminal, and this ground. The impedance Z1 seen from this 1st terminal maintaining equal relation substantially to the impedance Z2 seen from this 2nd terminal, so that the magnitude of attenuation between this 1st terminal and this 2nd terminal may be changed This switch attenuator is electrically controllable and it sets in this 2nd condition. It connects with this 3rd terminal, and this 1st terminal is intercepted from this 2nd terminal. This 2nd terminal Connect with a ground and this 4th terminal is intercepted from this 1st terminal, this 2nd terminal, this 3rd terminal, and this ground. The impedance Z1 seen from this 1st terminal maintaining equal relation substantially to the impedance Z3 seen from this 3rd terminal, so that the magnitude of attenuation between this 1st terminal and this 3rd terminal may be changed This switch attenuator is electrically controllable and it sets in this 3rd condition. It connects with this 2nd terminal, and this 4th terminal is intercepted from this 3rd terminal. This 3rd terminal Connect with a ground and this 1st terminal is intercepted from this 2nd

terminal, this 3rd terminal, this 4th terminal, and this ground. The impedance Z4 seen from this 4th terminal maintaining equal relation substantially to the impedance Z2 seen from this 2nd terminal, so that the magnitude of attenuation between this 4th terminal and this 2nd terminal may be changed. This switch attenuator is electrically controllable and it sets in this 4th condition. It connects with this 3rd terminal, and this 4th terminal is intercepted from this 2nd terminal. This 2nd terminal Connect with a ground and this 1st terminal is intercepted from this 2nd terminal, this 3rd terminal, this 4th terminal, and this ground. The impedance Z4 seen from this 4th terminal maintaining equal relation substantially to the impedance Z3 seen from this 3rd terminal, so that the magnitude of attenuation between this 4th terminal and this 3rd terminal may be changed. This switch attenuator is electrically controllable and the above-mentioned purpose is attained by that.

[0017] With a certain operation gestalt, the 1st transistor is prepared between said 1st terminal and grounds. The 2nd transistor is prepared between said 2nd terminal and grounds. The 3rd transistor is prepared between said 3rd terminal and grounds. The 4th transistor is prepared between this 1st terminal and this 2nd terminal. The 5th transistor It is prepared between this 1st terminal and this 3rd terminal, and the 6th transistor is prepared between said 4th terminal and grounds. The 7th transistor is prepared between this 2nd terminal and this 4th terminal, the 8th transistor is prepared between this 3rd terminal and this 4th terminal, and it sets in said 1st condition. This 3rd transistor is an ON state. This 5th transistor, this 6th transistor, this 7th transistor, and this 8th transistor It is an OFF state and sets in said 2nd condition. This 2nd transistor It is an ON state. This 4th transistor, this 6th transistor, this 7th transistor, and this 8th transistor It is an OFF state and sets in said 3rd condition. This 3rd transistor It is an ON state. This 1st transistor, this 4th transistor, this 5th transistor, and this 8th transistor It is an OFF state, and in said 4th condition, this 2nd transistor is an ON state and this 1st transistor, this 4th transistor, this 5th transistor, and this 7th transistor are OFF states.

[0018] With a certain operation gestalt, it is contained substantially [said impedances Z1 and Z4] in the range of $0.5 \times ZA - 2.0 \times ZA$, is contained substantially [said impedance Z2] in the range of $0.5 \times ZT - 2.0 \times ZT$, and is contained substantially [said impedance Z3] in the range of $0.5 \times ZR - 2.0 \times ZR$, and ZA, ZT, and ZR express the impedance of said antenna, said transmitter, and said receiver here, respectively.

[0019] With a certain operation gestalt, on the semi-conductor substrate, it integrates and is formed.

[0020] With a certain operation gestalt, it has power amplifier further, and this power amplifier is integrated and formed on said semi-conductor substrate.

[0021] With a certain operation gestalt, it has the low noise amplifier further, and this low noise amplifier is integrated and formed on said semi-conductor substrate.

[0022]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained, referring to a drawing. The same reference mark expresses the same component.

[0023] The "switch attenuator" in this specification says the equipment it has equipment and the function of RF switch for antennas, and RF attenuator so that it may mention later. Moreover, a "node" does not necessarily need the terminal for connection with the equipment exterior.

[0024] (Gestalt 1 of operation) Drawing 3 is the block diagram of the RF section 30 of the portable telephone with which the 1st operation gestalt of the switch attenuator of this invention is used. The switch attenuator 40 of this invention combines electrically an antenna 130, and power amplifier 116 or a low noise amplifier 152 according to the condition of transmission and reception. The switch attenuator 40 combines a node T1 with a node T2 electrically at the time of transmission, and, more specifically, combines node T3 with a ground electrically. Moreover, the switch attenuator 40 combines a node T1 with node T3 electrically at the time of reception, and combines a node T2 with a ground electrically. The ground in this specification is connected to the case shielded in RF while the negative electrode of a power source is connected and it offers common potential about the both sides of a direct-current (referred to as "DC" below) signal, and a RF signal. The flow of the signal at the time of the transmission and reception in the RF section 30 is the same as drawing 1 explained.

[0025] Since the switch attenuator 40 by this invention has a switch and the function of an attenuator so that it may mention later, it has the big effectiveness that the AGC amplifier 114 and attenuator 150 of drawing 1 can be lost. Moreover, if it manufactures as a semiconductor device which had the switch attenuator 40 unified, drastic reduction of size and cost is more desirable than a possible next door. In addition, all the transmission lines that connect each block of drawing 3 have the characteristic impedance of 50 ohms. Moreover, although the RF section 30 is used as some portable telephones, it is not limited to this here. The RF section 30 can be widely used for the equipment which transmits and receives a RF signal, and it can use the switch attenuator 40 widely as equipment to attenuate

while changing a RF signal.

[0026] In drawing 3, the control voltage generator valve flow coefficient 1 is generated based on the data in which the control voltage for setting up the condition of FET contained in the switch attenuator 40 as shown in Table 1 – 4 explained later was stored by the read only memory ROM 1, and is supplied to each FET. A read only memory ROM 1 stores the data for generating the control voltage of FET corresponding to the condition of Table 1 – 4.

[0027] Drawing 4 is the circuit diagram of the 1st operation gestalt of the switch attenuator by this invention. The switch attenuator 40 is equipped with nodes T1 and T2 and T3, and is connected to an antenna 130, power amplifier 116, and a low noise amplifier 152, respectively. The control voltage generator valve flow coefficient 1 generates the electrical potential difference which controls FET based on the data stored in the read only memory ROM 1, and outputs it to nodes CT1–CT5.

[0028] FET Q1 connects a node T1 to a ground with a certain impedance. The control voltage received in the node CT 1 minds resistance R12, and is FET. It is added to the gate of Q1 and is FET. This predetermined impedance of Q1 is changed. It responds to the control voltage of a node CT 1, and, specifically, is FET. Q1 can take the impedance of the large range from an ON state to an OFF state. FET In an ON state, the impedance of Q1 is low to extent it can consider that is zero, and high to extent it can consider that is infinite in an OFF state. FET Since it is the depletion type of N type, Q1 is FET. It is FET conversely that what is necessary is just to give the electrical potential difference Vgs between the gate sources more than 0 [V] in order to make Q1 into an ON state. What is necessary is just to give the electrical potential difference Vgs between the gate sources below a threshold VTH [V] ($VTH < 0$), in order to make Q1 into an OFF state. FET When filling the relation which the electrical potential difference Vgs between the gate sources of Q1 becomes $VTH < Vgs < 0$, it sets on these specifications, and it is FET. Q1 is made to call that it is the "intermediate state" of an ON state and an OFF state. FET Q1 is the Schottky barrier gate mold FET (referred to as "MESFET" below) with the gestalt of this operation. As mentioned above, FET It sets on these specifications and the explanation about Q1 is FET. It is applied also about Q2–Q4.

[0029] FET It is FET like Q1. Q2 and Q3 connect a node T2 and T3 to a ground with a certain impedance, respectively. The control voltage received in nodes CT2 and CT3 minds resistance R22, and is FET, respectively. Resistance R32 is minded [of Q2] again, and it is FET. It is added to the gate of Q3 and is FET, respectively. The impedance of Q2 and Q3 is changed. Resistance R12, R22, and R32 is resistance for gate bias.

[0030] FET Between the source of Q1, Q2, and Q3, and a ground, resistance R11, R21, and R31 is formed, respectively. These resistance R11, R21, and R31 is FET, respectively. Impedance matching is taken by adjusting the nodes T1 and T2 in case Q1, Q2, and Q3 are ON states, and the impedance between T3 and a ground.

[0031] FET It is FET like Q1. Q4 and Q5 connect a node T2 and T3 to a node T1 with a certain impedance, respectively. The control voltage received in nodes CT4 and CT5 minds resistance R42, respectively, and is FET. Resistance R52 is minded [of Q4] again, and it is FET. It is added to the gate of Q5 and the impedance of FETQ4 and Q5 is changed, respectively.

[0032] Next, actuation of the switch attenuator 40 is explained. The switch attenuator 40 has the following modes of operation 1–4. Namely, transmission without mode 1:attenuation, transmission with mode 2:attenuation, the reception without mode 3:attenuation, and the mode 4: It is reception with attenuation. Attenuation between a node T1, and a node T2 or node T3 of "attenuation" is said here. For example, in the mode 1, attenuation between a node T1 and a node T2 does not exist. The mode 1 is used when the migration terminal containing the RF section 30 is distant from the base station (i.e., when supplying an antenna 130, without attenuating the RF signal outputted from power amplifier 116). The mode 2 is used when the migration terminal which contains the RF section 30 conversely is close to a base station (i.e., since the RF signal outputted from power amplifier 116 is attenuated when supplying an antenna 130). It is applied also when it is reception that it is the same as that of the case of transmission. The mode 3 is used when the migration terminal containing the RF section 30 is distant from the base station (i.e., when supplying a low noise amplifier 152, without attenuating the RF signal inputted from the antenna 130). The mode 4 is used when the migration terminal which contains the RF section 30 conversely is close to a base station (i.e., since the RF signal inputted from the antenna 130 is attenuated when supplying a low noise amplifier 152).

[0033] The switch attenuator 40 of this invention can change the magnitude of attenuation of the switch attenuator 40 continuously by changing the control voltage of a switching element (here FET) in the mode 2 and the mode 4 so that it may mention later. Consequently, the switch attenuator of this invention does big effectiveness so in the mobile communication which can take a range with large output power at the time of transmission and input power at the time of reception.

[0034] (Mode 1) FET of the switch attenuator 40 in the mode 1 The condition of Q1–Q5 is shown in Table 1.

[0035]

[Table 1]

FET	Q1	Q2	Q3	Q4	Q5
状態	オフ	オフ	オン	オン	オフ

[0036] It is FET in order to realize the mode 1 of the switch attenuator 40. What is necessary is just to impress the control voltage corresponding to each condition of setting Q1–Q5 as the condition which shows in Table 1 to nodes CT1–CT5. It is FET as mentioned above. It is FET that what is necessary is just to apply the electrical potential difference for example, more than 0 [V] to each gate in order to make Q1–Q5 into an ON state. What is necessary is just to apply the electrical potential difference for example, below VTH [V] to each gate, in order to make Q1–Q5 into an OFF state.

[0037] Drawing 5 is the representative circuit schematic of the switch attenuator 40 in the mode 1. In drawing 5, the closed switch expresses FET of an ON state and the open switch expresses FET of an OFF state. As the mode 1 is shown in drawing 5, an impedance is mostly connected to a node T2 by zero, as for node T3, an impedance is mostly connected to a ground by zero, and node T3 is intercepted for the node T1 from the node T1 and the node T2. Therefore, the RF signal outputted from power amplifier 116 in the mode 1 is FET, without receiving and decreasing in a node T2. An antenna 130 is supplied through Q4 and a node T1. Moreover, node T3 which is an input terminal to a low noise amplifier 152 is FET. It prevents Q's3 connecting with a ground and an unnecessary RF signal being inputted by that cause into a low noise amplifier 152.

[0038] The insertion loss of the switch attenuator 40 in the mode 1 is FET. It is only about 0.5dB resulting from the impedance (that is, impedance equivalent to on resistance) of the ON state of Q4.

[0039] (Mode 2) FET of the switch attenuator 40 in the mode 2 The condition of Q1–Q5 is shown in Table 2.

[0040]

[Table 2]

FET	Q1	Q2	Q3	Q4	Q5
状態	中間	中間	オン	中間	オフ

[0041] It is FET in order to realize the mode 2 of the switch attenuator 40. What is necessary is just to impress the control voltage corresponding to each condition of setting Q1–Q5 as the condition which shows in Table 2 to nodes CT1–CT5. In the mode 2 and the mode 4, FET is used by the intermediate state. FET What is necessary is just to apply to each gate the electrical potential difference which becomes $0 < V_{gs} < V_{TH}$ as an electrical potential difference V_{gs} between the gate sources, in order to make Q1–Q5 into an intermediate state.

[0042] Drawing 6 is the representative circuit schematic of the switch attenuator 40 in the mode 2. In drawing 6, the closed switch expresses FET of an ON state, the open switch expresses FET of an OFF state, and resistance expresses FET of an intermediate state. Hereafter, the impedance of FETQ1–Q5 of an intermediate state is made to express like ZQ1–ZQ5, respectively. As the mode 2 is shown in drawing 6, it connects with a node T2 with an impedance ZQ4, and a node T1 is connected to a ground with an impedance ZQ1. A node T2 is connected to a ground with an impedance ZQ2. As for node T3, an impedance is mostly connected to a ground by zero, and node T3 is intercepted from the node T1 and the node T2. Therefore, it is received in a node T2, it is accompanied by the desired magnitude of attenuation, and the RF signal outputted from power amplifier 116 in the mode 2 is FET. An antenna 130 is supplied through Q1, Q2, Q4, and a node T1. Moreover, node T3 which is an input terminal to a low noise amplifier 152 is FET. It prevents Q's3 connecting with a ground and an unnecessary RF signal being inputted by that cause into a low noise amplifier 152.

[0043] The magnitude of attenuation of the switch attenuator 40 in the mode 2 is FET. It changes changing the control voltage applied to the gate of Q1, Q2, and Q4, i.e., by changing impedances ZQ1, ZQ2, and ZQ4. The value of the control voltage applied to the gate of FETQ1, Q2, and Q4 is beforehand stored in the read only memory ROM 1, for example, and is read according to the required magnitude of attenuation. For example, if the control voltage generator valve flow coefficient 1 which is a programmable voltage generator generates control voltage based on the data showing the control voltage read from ROM1 and outputs to the gate of each FET, the mode 2 and the mode 4 only for a desired amount to attenuate a RF signal are realizable. Moreover, ROM1 is FET. The data showing the control voltage (that is, the electrical potential difference more than each 0 [V] and the electrical potential difference below VTH [V]) applied to the gate of Q3 and Q5 may be stored collectively. Furthermore, it sets in the modes 1, 3,

and 4, and ROM1 is FET. The data showing the control voltage applied to Q1–Q5 may be stored collectively.

[0044] (Mode 3) FET of the switch attenuator 40 in the mode 3 The condition of Q1–Q5 is shown in Table 3.

[0045]

[Table 3]

FET	Q1	Q2	Q3	Q4	Q5
状態	オフ	オン	オフ	オフ	オン

[0046] It is FET in order to realize the mode 3 of the switch attenuator 40. What is necessary is just to impress the control voltage corresponding to each condition of setting Q1–Q5 as the condition which shows in Table 3 to nodes CT1–CT5.

[0047] Drawing 7 is the representative circuit schematic of the switch attenuator 40 in the mode 3. As the mode 3 is shown in drawing 7 R> 7, an impedance is mostly connected to node T3 by zero, mostly, an impedance is connected to a ground by zero and the node T2 is intercepted [the node T2] for the node T1 from a node T1 and node T3. Therefore, the RF signal inputted from the antenna 130 in the mode 3 is FET, without receiving and decreasing in a node T1. A low noise amplifier 152 is supplied through Q5 and node T3. Moreover, the node T2 which is an output terminal from power amplifier 116 is FET. It prevents Q's2 connecting with a ground and an unnecessary RF signal being outputted by that cause to a low noise amplifier 152.

[0048] The insertion loss of the switch attenuator 40 in the mode 3 is FET. It is only about 0.5dB resulting from the impedance of the ON state of Q5.

[0049] (Mode 4) FET of the switch attenuator 40 in the mode 4 The condition of Q1–Q5 is shown in Table 4.

[0050]

[Table 4]

FET	Q1	Q2	Q3	Q4	Q5
状態	中間	オン	中間	オフ	中間

[0051] It is FET in order to realize the mode 4 of the switch attenuator 40. What is necessary is just to impress the control voltage corresponding to each condition of setting Q1–Q5 as the condition which shows in Table 4 to nodes CT1–CT5.

[0052] Drawing 8 is the representative circuit schematic of the switch attenuator 40 in the mode 4. As the mode 4 is shown in drawing 8 R> 8, it connects with node T3 with an impedance ZQ5, and a node T1 is connected to a ground with an impedance ZQ1. Node T3 is connected to a ground with an impedance ZQ3. Mostly, an impedance is connected to a ground by zero, and the node T2 is intercepted for the node T2 from a node T1 and node T3. Therefore, it is received in a node T1, it is accompanied by the desired magnitude of attenuation, and the RF signal inputted from the antenna 130 in the mode 4 is FET. A low noise amplifier 152 is supplied through Q1, Q3, Q5, and node T3. Moreover, the node T2 which is an output terminal from power amplifier 116 is FET. It prevents Q's2 connecting with a ground and an unnecessary RF signal being inputted by that cause into a low noise amplifier 152.

[0053] The magnitude of attenuation of the switch attenuator 40 in the mode 4 is FET. It changes changing the control voltage applied to the gate of Q1, Q3, and Q5, i.e., by changing impedances ZQ1, ZQ3, and ZQ5. The value of the control voltage applied to the gate of FETQ1, Q3, and Q5 is beforehand stored in the read only memory ROM 1, as explained in the mode 2, and it is read according to the required magnitude of attenuation.

[0054] The magnitude of attenuation can be changed filling the relation it is substantially unrelated $ZT1=ZT2=Z0$ in the mode 2 according to the gestalt of the 1st operation. An impedance ZT1 expresses the impedance of the switch attenuator 40 seen from the node T1, an impedance ZT2 expresses the impedance of the switch attenuator 40 seen from the node T2, and an impedance Z0 expresses the characteristic impedance (for example, 50ohms) of the circuit connected outside here. The magnitude of attenuation can be changed filling similarly the relation it is substantially unrelated $ZT1=ZT3=Z0$ in the mode 4 according to the gestalt of the 1st operation. An impedance ZT3 expresses the impedance of the switch attenuator 40 seen from node T3 here.

[0055] Moreover, even if above-mentioned $ZT1=ZT2=Z0$ and the relation it is unrelated $ZT1=ZT3=Z0$ are not filled, it is desirable that relation called $0.5xZA \leq ZT1 \leq 2.0xZA$, $0.5xZT \leq ZT2 \leq 2.0xZT$, and $0.5xZR \leq ZT3 \leq 2.0xZR$ is filled. An impedance ZA expresses the characteristic impedance of the circuit (here antenna 130) connected to a node T1, an impedance ZT expresses the characteristic impedance of the circuit (here power amplifier 116) connected to a node T2, and an impedance ZR expresses the characteristic impedance of the circuit (here low noise amplifier 152)

connected to node T3 here.

[0056] Drawing 9 is the top view of the switch attenuator 40 of this invention integrated and formed on the semiconductor substrate. As shown in drawing 9, the switch attenuator 40 is integrated and formed on the gallium-arsenide (referred to as "GaAs" below) substrate 901. "GND" of drawing 9 expresses a ground and other reference marks correspond with them in drawing 4. FET Q1-Q5 are MESFET(s), and they are formed by ion-implantation on the GaAs substrate 901. FET Gate length is 0.5 micrometers and the gate width of the size of Q1-Q5 is 800 micrometers. The closure of the semiconductor chip which realized the switch attenuator 40 shown in drawing 9 is carried out to the resin mold package of ten pins, and it is made available.

[0057] (Gestalt 2 of operation) Drawing 10 is the circuit diagram of the 2nd operation gestalt of the switch attenuator by this invention. FET of drawing 10 Q1D, Q2D, Q3D, Q4D, and Q5D are dual gate FET. FET The gate bias resistors R13 and R14, R23 and R24, R33 and R34, R43 and R44, and R53 and R54 are connected to the 1st gate and the 2nd gate of Q1 D-Q5D, respectively. Moreover, FET Between the 2nd gate of Q1D – Q5D, and a drain, capacitors C13, C23, C33, C43, and C53 are connected, respectively, and it is FET. Between the 1st gate of Q1 D-Q5D, and the source, capacitors C14, C24, C34, C44, and C54 are connected, respectively.

[0058] As for the 2nd operation gestalt, it differs from the 1st operation gestalt that the capacitor is connected between that dual gate FET is used instead of, and a drain and the 2nd gate and between the source and the 1st gate. [a single gate FET] According to the configuration of the 2nd operation gestalt, the nonlinearity which FET has can be reduced and the outstanding distorted property can be realized.

[0059] (Gestalt 3 of operation) Drawing 11 is the block diagram of the RF section 1100 of the portable telephone with which the 3rd operation gestalt of the switch attenuator of this invention is used. The switch attenuator 1200 of this invention combines electrically antennas 130 or 131, and power amplifier 116 or a low noise amplifier 152 according to the condition of transmission and reception.

[0060] More specifically, the switch attenuator 1200 intercepts the node which one is electrically combined with a node T2 of a node T1 and the T four at the time of transmission, combines node T3 with a ground electrically, and is not combined with a node T2 among a node T1 and T four from other nodes and grounds.

[0061] Moreover, the switch attenuator 1200 intercepts the node which one is electrically combined with node T3 of a node T1 and the T four at the time of reception, combines a node T2 with a ground electrically, and is not combined with node T3 among a node T1 and T four from other nodes and grounds. Unlike having used the antenna with the 1st single operation gestalt, the 3rd operation gestalt can use two antennas 130 and 131. Therefore, in addition to the effectiveness of the 1st operation gestalt, the 3rd operation gestalt has the effectiveness that two antennas 130 and 131 can be alternatively used according to the situation of transmission and reception. The configuration of this 3rd operation gestalt enables for example, space diversity transmission and reception. In addition, all the transmission lines that connect each block of drawing 11 have the characteristic impedance of 50 ohms.

[0062] The control voltage generator valve flow coefficient 2 in drawing 11 and drawing 12 and a read only memory ROM 2 function as the control voltage generator valve flow coefficient 1 and a read only memory ROM 1 similarly except for the nodes which supply the electrical potential difference which controls FET being CT1-CT8.

[0063] Drawing 12 is the circuit diagram of the 3rd operation gestalt of the switch attenuator by this invention. In order to join together electrically of a node T2 and T3 to one, the switch attenuator 1200 adds node T four to the component of the switch attenuator 40, and is FET. It has further Q6-Q8, the resistance R62, R72, and R82 for gate bias, nodes CT6-CT8, and the resistance R61 for impedance matching.

[0064] Next, actuation of the switch attenuator 1200 is explained. The switch attenuator 1200 has the following modes of operation 1-8. Namely, the transmission without attenuation using the mode 1:antenna 130, the mode 2 : The transmission with attenuation using an antenna 130, Mode 3 : The reception without attenuation using an antenna 130, the reception with attenuation using the mode 4:antenna 130, mode 5: -- they are the transmission without attenuation using an antenna 131, the transmission with attenuation using the mode 6:antenna 131, the reception without attenuation using the mode 7:antenna 131, and reception with attenuation using the mode 8:antenna 131. The modes 1-4 of the 3rd operation gestalt are equivalent to the mode 1 of the 1st operation gestalt - the mode 4, respectively. Node T four of the modes 5-8 of the 3rd operation gestalt is the same as that of the modes 1-4 except for being electrically combined with a node T2 or T3 instead of a node T1.

[0065] What is necessary is just to impress the control voltage corresponding to each condition of setting FETQ1-Q8 as the condition which shows in following Table 5 – 12, respectively to nodes CT1-CT8, in order to realize the modes 1-8 of the switch attenuator 1200. The representative circuit schematic in the mode 1 of the switch

attenuator 1200 – the mode 8 is shown in drawing 13 – drawing 20 , respectively.

[0066]

[Table 5]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オフ	オン	オン	オフ	オフ	オフ	オフ

[0067]

[Table 6]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	中間	中間	オン	中間	オフ	オフ	オフ	オフ

[0068]

[Table 7]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オン	オフ	オフ	オン	オフ	オフ	オフ

[0069]

[Table 8]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	中間	オン	中間	オフ	中間	オフ	オフ	オフ

[0070]

[Table 9]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オフ	オン	オフ	オフ	オフ	オン	オフ

[0071]

[Table 10]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	中間	オン	オフ	オフ	中間	中間	オフ

[0072]

[Table 11]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オン	オフ	オフ	オフ	オフ	オフ	オン

[0073]

[Table 12]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オン	中間	オフ	オフ	中間	オフ	中間

[0074] With the gestalt of the 3rd operation, the magnitude of attenuation can be changed like the gestalt of the 1st operation, filling substantially $ZT1=ZT2=Z0$ and the relation it is unrelated $ZT1=ZT3=Z0$ in the modes 2 and 4, respectively. Moreover, with the gestalt of the 3rd operation, the magnitude of attenuation can be changed in the modes 6 and 8, filling substantially $ZT4=ZT2=Z0$ and the relation it is unrelated $ZT4=ZT3=Z0$, respectively. An impedance $ZT4$ expresses the impedance of the switch attenuator 1200 seen from node T four here.

[0075] Moreover, even if the above-mentioned $ZT1=ZT2=Z0$, $ZT1=ZT3=Z0$, $ZT4=ZT2=Z0$, and the relation it is unrelated $ZT4=ZT3=Z0$ are not filled, it is desirable that relation called $0.5xZA \leq ZT1 \leq 2.0xZA$, $0.5xZT \leq ZT2 \leq 2.0xZT$, $0.5xZR \leq ZT3 \leq 2.0xZR$, and $0.5xZB \leq ZT4 \leq 2.0xZB$ is filled. An impedance ZB expresses the characteristic impedance of the circuit (here antenna 131) connected to node T four here.

[0076] With the gestalt of the 1st explained above – the 3rd operation, by setting FET as the middle condition of ON

and OFF, also when the property of the circuit connected to a switch attenuator changes, it can respond flexibly. Such property change of the circuit connected may take place, when changing the power outputted from the power amplifier for transmission.

[0077] Although a desired characteristic impedance is obtained with the gestalt of the above-mentioned implementation in the frequency band used, for example by the communication link between a portable telephone and a base station, it is not limited to this frequency band, but can apply to RF band widely.

[0078] Based on the indication of the gestalt of the 2nd operation, the further effectiveness that the outstanding distorted property is realizable can also be acquired by transposing FET of the gestalt of the 3rd operation to dual gate FET.

[0079] FET used for the switch attenuator of this invention is not limited to a depletion type, but an enhancement type may be used for it. Moreover, FET should just be the device which is not limited to this although it is MESFET, but can control an impedance by the above-mentioned operation gestalt electrically with the control terminal. As long as conditions, such as an operating frequency and parasitic capacitance of a device proper, allow, a PIN diode, the PN-junction mold FET, a MOSFET, etc. may be used, for example.

[0080] Moreover, if the switch attenuator by this invention is integrated and formed on a semi-conductor substrate with power amplifier or a low noise amplifier, reduction of size and cost can be aimed at and it is more desirable.

[0081] The control voltage generators valve flow coefficient1 and valve flow coefficient2 and read only memories ROM1 and ROM2 will not be restricted to the configuration explained with the gestalt of the above-mentioned implementation, if the control voltage for setting the condition of FET of the switch attenuator by this invention as the condition of either an ON state, an intermediate state and an OFF state can be generated. For example, a programmable voltage generator without the memory which stores data in digital one may be used. Moreover, random access memory may be used instead of read only memories ROM1 and ROM2.

[0082] As shown in Table 2, Table 4, Table 6, and Table 8, 10, and 12, with the gestalt of above-mentioned operation, three FET is set as an intermediate state at the time of the transmission with attenuation, or reception. However, the number of FET of an intermediate state is not restricted to three pieces, but when at least one FET is an intermediate state, the desired magnitude of attenuation should just be obtained.

[Translation done.]

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- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
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- 3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram of the radio-frequency head 10 of the transceiver circuit by the Prior art.
[Drawing 2] It is the circuit diagram of the switch 20 by the Prior art.
[Drawing 3] It is the block diagram of the RF section 30 of the portable telephone with which the 1st operation gestalt of the switch attenuator of this invention is used.
[Drawing 4] It is the circuit diagram of the 1st operation gestalt of the switch attenuator by this invention.
[Drawing 5] It is the representative circuit schematic of the switch attenuator 40 in the mode 1.
[Drawing 6] It is the representative circuit schematic of the switch attenuator 40 in the mode 2.
[Drawing 7] It is the representative circuit schematic of the switch attenuator 40 in the mode 3.
[Drawing 8] It is the representative circuit schematic of the switch attenuator 40 in the mode 4.
[Drawing 9] It is the top view of the switch attenuator 40 of this invention integrated and formed on the semi-conductor substrate.
[Drawing 10] It is the circuit diagram of the 2nd operation gestalt of the switch attenuator by this invention.
[Drawing 11] It is the block diagram of the RF section 1100 of the portable telephone with which the 3rd operation gestalt of the switch attenuator of this invention is used.
[Drawing 12] It is the circuit diagram of the 3rd operation gestalt of the switch attenuator by this invention.
[Drawing 13] It is the representative circuit schematic of the switch attenuator 1200 in the mode 1.
[Drawing 14] It is the representative circuit schematic of the switch attenuator 1200 in the mode 2.
[Drawing 15] It is the representative circuit schematic of the switch attenuator 1200 in the mode 3.
[Drawing 16] It is the representative circuit schematic of the switch attenuator 1200 in the mode 4.
[Drawing 17] It is the representative circuit schematic of the switch attenuator 1200 in the mode 5.
[Drawing 18] It is the representative circuit schematic of the switch attenuator 1200 in the mode 6.
[Drawing 19] It is the representative circuit schematic of the switch attenuator 1200 in the mode 7.
[Drawing 20] It is the representative circuit schematic of the switch attenuator 1200 in the mode 8.

[Description of Notations]

40 Switch Attenuator

Q1, Q2, Q3, Q4, Q5 FET

R11, R12, R21, R22, R31, R32, R42, R52 Resistance

T1, T2, T3, CT1, CT2, CT3, CT4, CT5 Node

130 Antenna

[Translation done.]

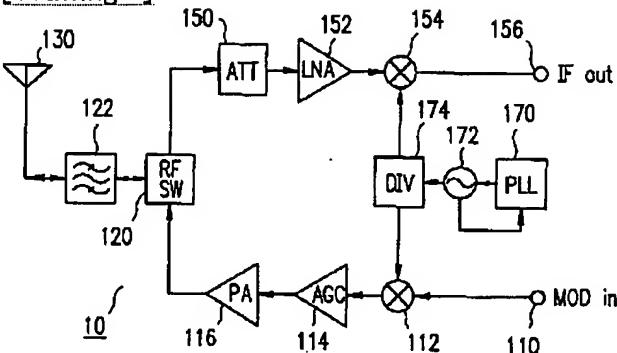
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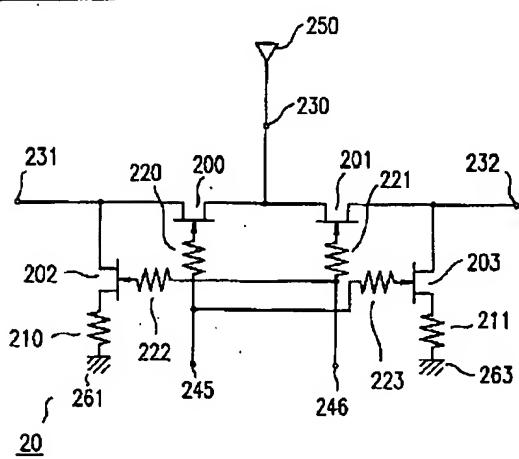
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DRAWINGS

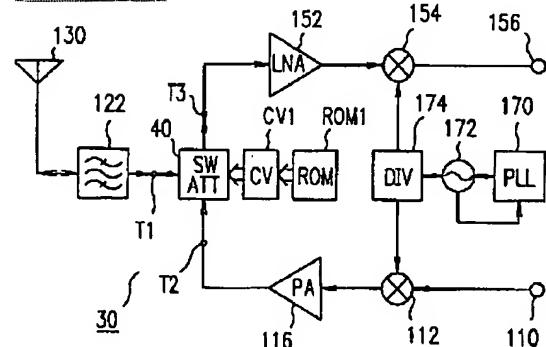
[Drawing 1]



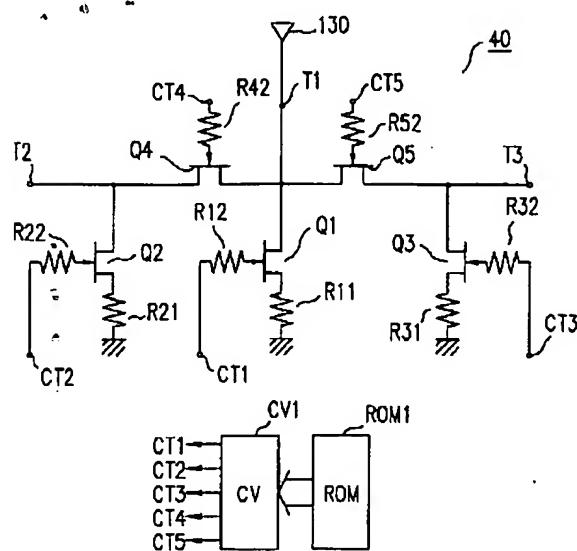
[Drawing 2]



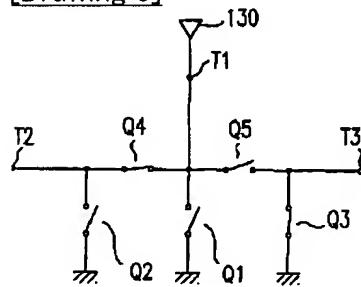
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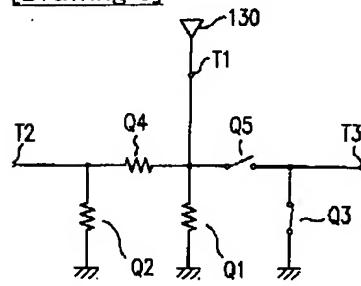
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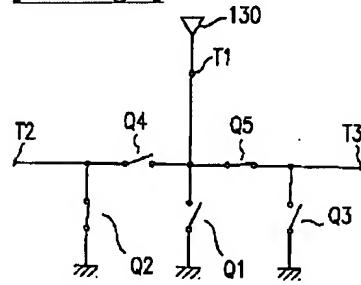
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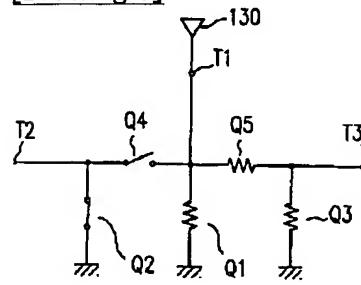
[Drawing 6]

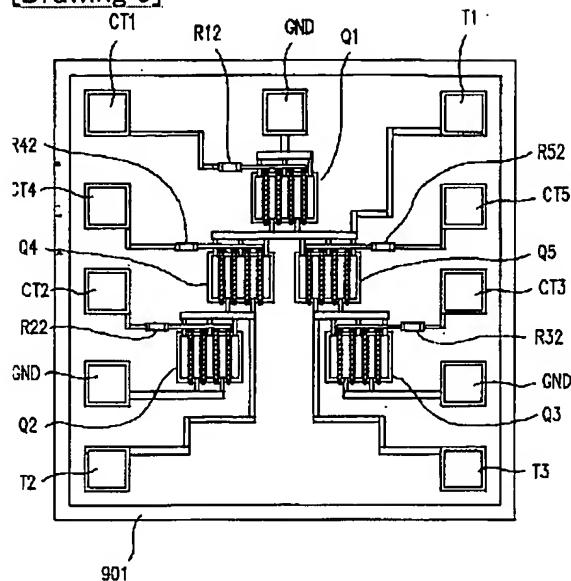
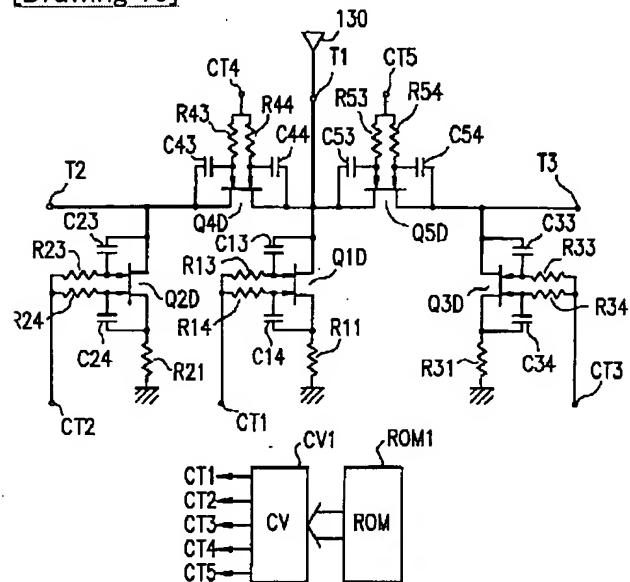
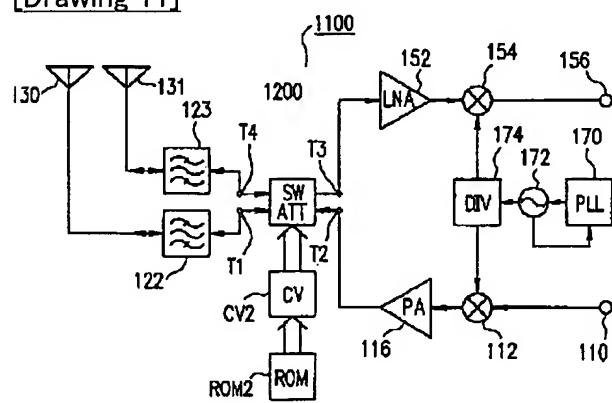


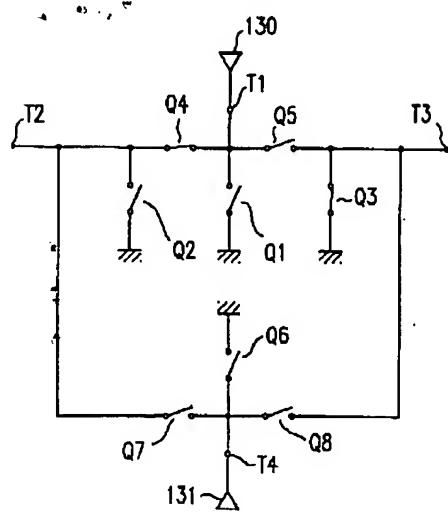
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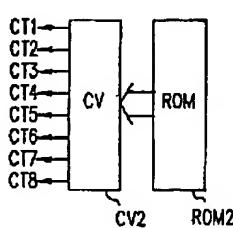
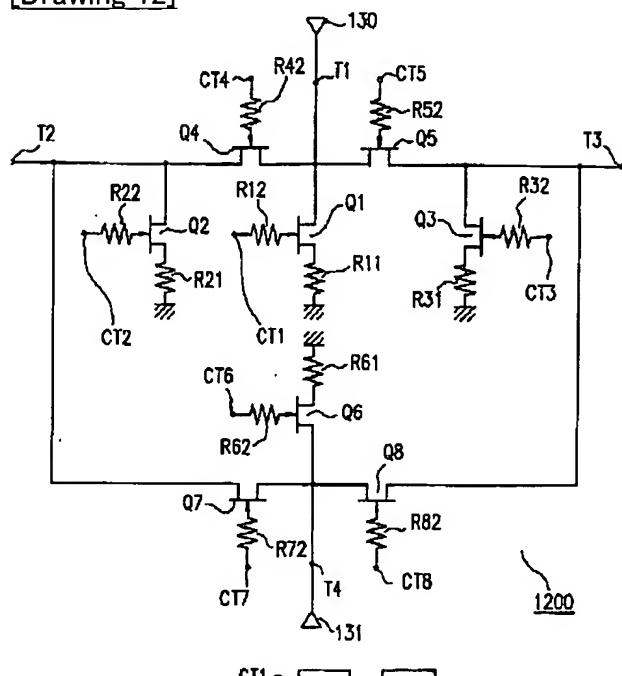
[Drawing 8]



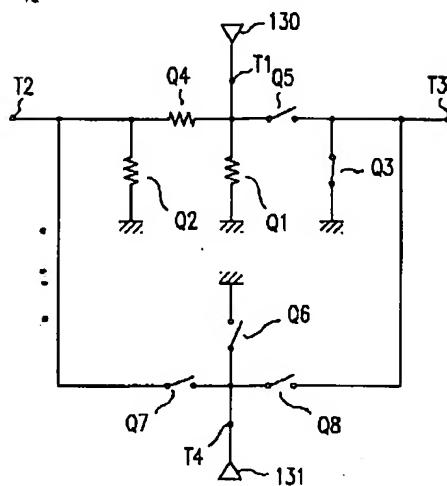
[Drawing 9][Drawing 10][Drawing 11][Drawing 13]



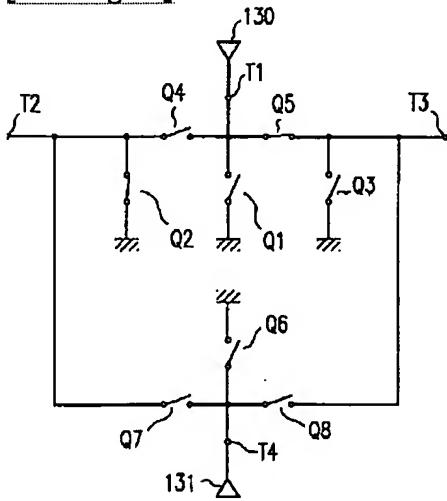
[Drawing 12]



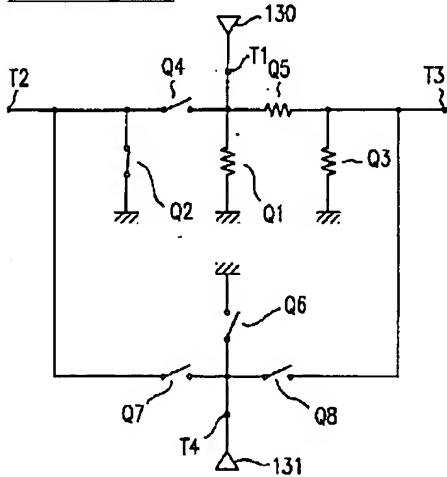
[Drawing 14]



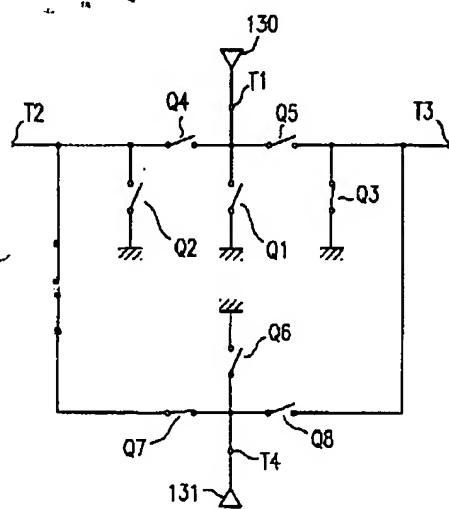
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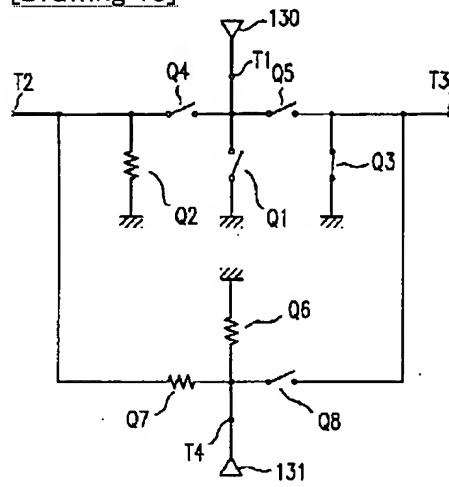
[Drawing 16]



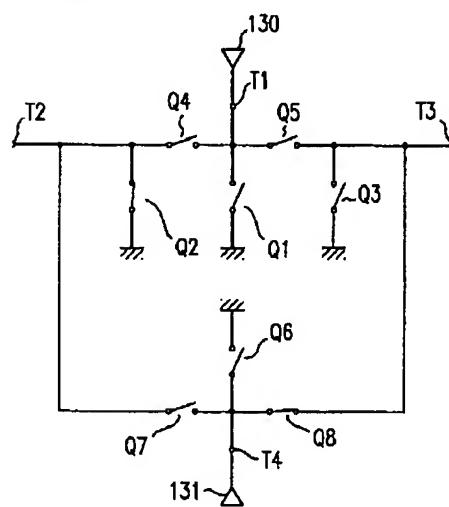
[Drawing 17]



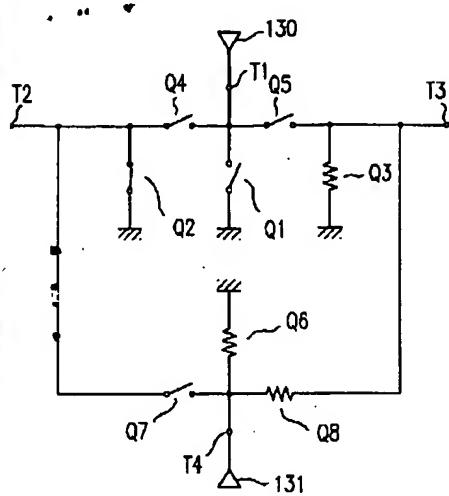
[Drawing 18]



[Drawing 19]



[Drawing 20]



[Translation done.]